

YC13XX Product Brief

High Performance Low Power BR/BLE 5.2 SoC

Preliminary Datasheet

General Descriptions

The YC13XX is a high performance, low power System-on-Chip (SoC) integrating a Bluetooth® 5.2 compliant 2.4-GHz transceiver, 24 MHz proprietary 32 bit MCU with a RAM of 12 KB and eFuse of 512 bits.

The YC13XX supports Bluetooth Basic Rate, Bluetooth Low Energy and Bluetooth 5.2 features including high-throughput 2 Mbps, Long Range and the Direction Finding. It can be paired through HCI interface with a more powerful MCU for applications requiring advanced wireless connectivity.

The fully-featured multiprotocol radio, +12 dBm output power, -99 dBm sensitivity and extended temperature range of -40 to 110°C makes it suitable for lighting applications.

The YC13XX features built-in USB, proprietary 32-bit MCU clocked at 24 MHz, integrated capless LDOs supporting 1.7-5.5V supply range, making it a perfect microcontroller for cost-sensitive applications such as mouse devices, toys and disposables.

Key Features

- MCU subsystems
 - 24 MHz 32-bit proprietary MCU for system control and PHY/link layer management
 - AES128 HW encryption
 - Serial wire debug
- Memories
 - 512 bit eFuse
 - 12 kB data RAM
 - 4 kB RAM supporting retention mode
- Radio transceiver
 - BR/Bluetooth 5.2/Long Range
 - +12 dBm TX power in 1dB/steps
 - -99 dBm RX sensitivity @ BLE 1 Mbps
 - -96 dBm RX sensitivity @ BLE 2 Mbps
 - Integrated balun with single-ended output and direct connection to antenna
 - 5.8 mA RX system current @ BLE 1 Mbps -99 dBm sensitivity (3V DC-DC 90% efficiency)
 - 5.2 mA RX system current @ BLE 1 Mbps -97 dBm sensitivity (3V DC-DC 90% efficiency)
 - 10.9 mA TX system current (3V DC-DC 90% efficiency, 0 dBm)
- Power management
 - Always-On (AON) supply: 1.7~ 5.5V
 - Main supply: 1.3 ~ 5.5V supporting external DCDC through a dedicated wakeup pin
 - Integrated LDOs requiring no external decoupling capacitors
 - 3.3V 40 mA capless LDO
 - 1.3 μ A in sleep mode (wake on RTC, no RAM retention)
 - 2 μ A in sleep mode (wake on RTC, 4 KB RAM retention)
- Clock generation
 - Dedicated PLL to support 16M/24M/26M/32M crystals
 - Crystal trimming
 - 40 MHz RC oscillator for fast wakeup
 - Low jitter low power 32 KHz RC oscillator
- 10-channel 10-bit ADC
- Digital peripherals
 - Up to 20 GPIOs w/ functions fully multiplexed
 - Two-wire master (I²C compatible) up to 600 kbps
 - 2 x UART(RTS/CTS) with HCI-H5 protocol up to 3.25 Mbps
 - 2 x SPI Master/Slave up to 24 Mbps
 - 1-axis Quadrature Decoder
 - 12 Mbps Full Speed USB 2.0
- Temperature range: -40°C to +110°C

Applications

- Mouse devices
- Toys
- Lightning applications
- Disposables
- Commercial and industrial applications requiring advanced connectivity

Key Benefits

- Best-in-class sensitivity and output power for RF-demanding applications
- BR for enhanced interoperability
- Lowest system cost for cost-oriented designs

Block Diagram

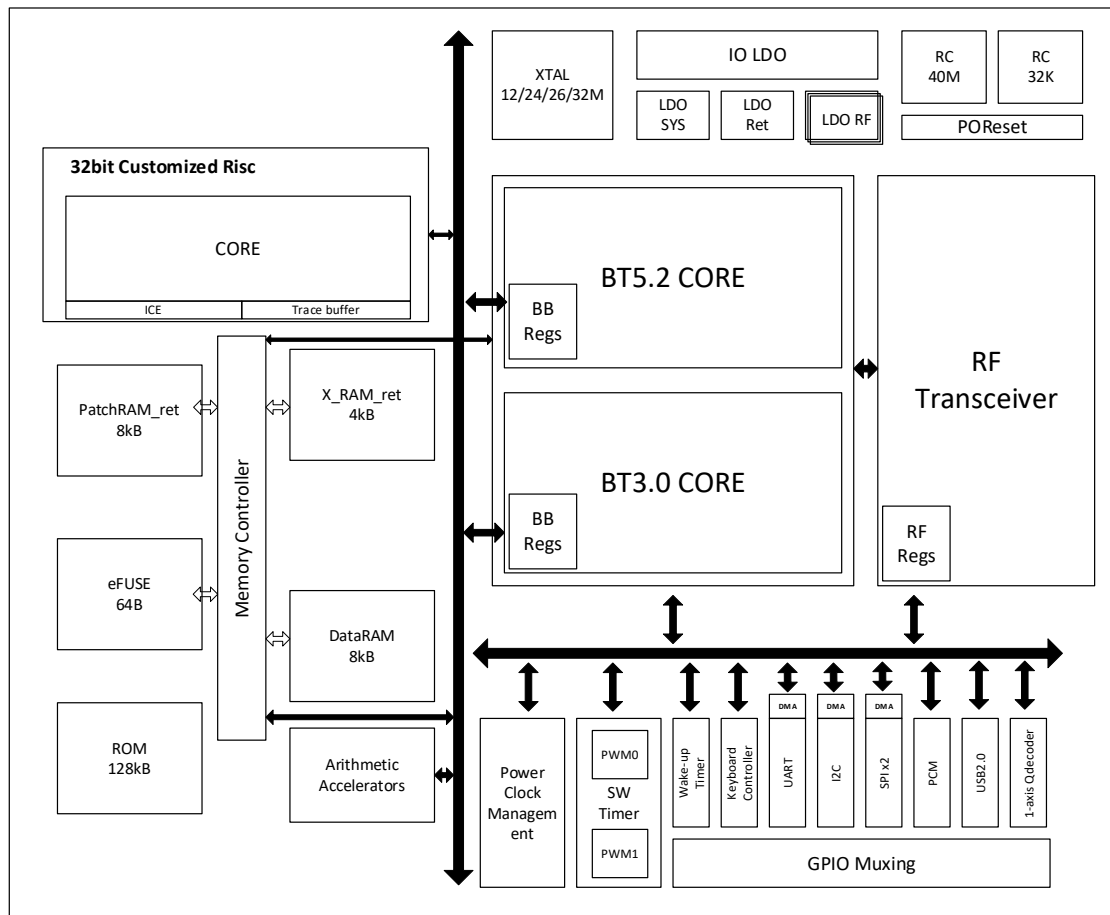


Figure 0-1 Block diagram

Pinout Information

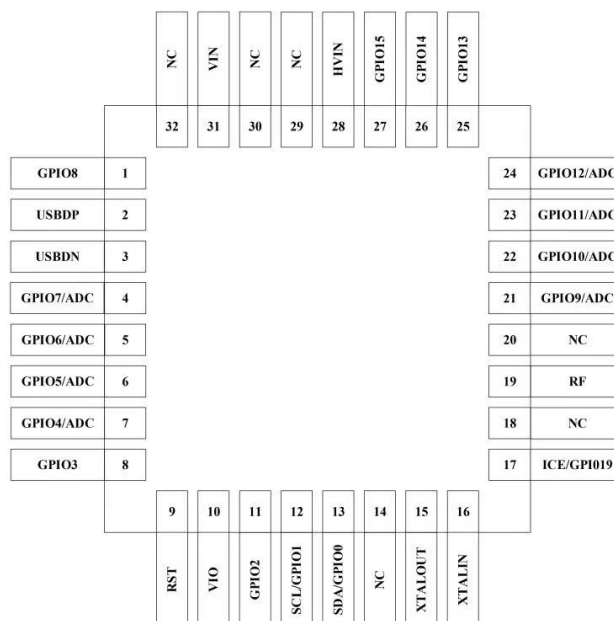


Figure 0-1 Pinout top view (QFN32 package)

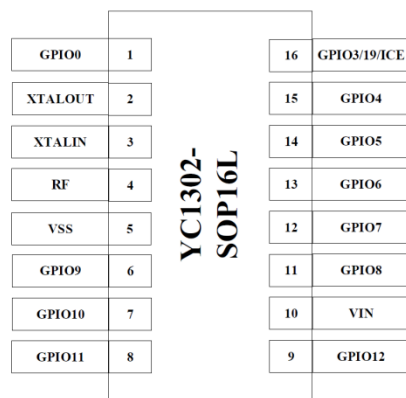


Figure 0-2 Pinout top view (SOP16 package)

Abbreviations:

PWR: Power pin

AIO: Analog IO pin

DIO: Digital IO pin

RF: RF IO pin

Table 0-1 Pinout Information

Pin Number		Type	Name	Description
QFN32	SOP16			
1			GPIO8	Refer to Table 0-2
2		DIO	USBDP	USB port.
3		DIO	USBDN	USB port.
4	12	DIO	GPIO7/ADC	Refer to Table 0-2
5	13	DIO	GPIO6/ADC	
6	14	DIO	GPIO5/ADC	
7		DIO	GPIO4/ADC	
8		DIO	GPIO3	
9		DIO	RSTN	Global reset, active low. OR gated with internal POR. NC if not needed.
10		PWR	VIO	I/O power, 1.8~3.6V, no external capacitor needed
11	15	DIO	GPIO2	Refer to Table 0-2
12		DIO	GPIO1/SCL	Internal pull up 1Kohm to VIO and no need external pull up resistor.
13	1	DIO	GPIO0/SDA	Internal pull up 1Kohm to VIO and no need external pull up resistor.
14			NC	
15	2	AIO	XTALOUT	XTAL port
16	3	AIO	XTALIN	XTAL port, or external reference clock input
17	16	DIO	ICE/GPIO19	debug port, Tx & Rx
18			NC	
19	4	RF	RF	ANT port
20			NC	NC
21	6	DIO	GPIO9/ADC/EXEN	Refer to Table 0-2
22	7	DIO	GPIO10/ADC	
23	8	DIO	GPIO11/ADC	
24	9	DIO	GPIO12/ADC	
25		DIO	GPIO13	
26		DIO	GPIO14	
27		DIO	GPIO15	
28		PWR	HVIN	Always-on power input, 1.55~5.5V, 1μF bypass cap
29			NC	
30			NC	
31	10	PWR	VIN	Main power input, 1.25~5.5V, 1μF bypass cap
32			NC	
	5	GND	VSS	GND
	11	DIO	GPIO8	Refer to Table 0-2

Note 1 : Drive capability of GPIO[19:2] is up to 100mA,GPIO[1:0] internal pullup & pulldown resistance is 1kohm.

Note 2 : GPIO[9] is by default not gpio function, and is in output high level status after por, which is used as external BUCK enable signal. GPIO[9] will restore gpio function by setting lpm_ctrl[52] to 0.

Note 3 : GPIO[9] can not used as lpm wakeup source.

Note 4 : GPIO[19] is by default in pullup status as ice function after por. GPIO[19] will restore gpio function by setting ice_mode to 0.

Table 0-2 GPIO Multiplexing

Pin Name	boot function	function-analog
GPIO[0]		atest[5]
GPIO[1]		atest[4]
GPIO[2]		atest[7]
GPIO[3]		atest[6]
GPIO[4]		saradc [0]
GPIO[5]		saradc [1]
GPIO[6]		saradc [2]
GPIO[7]		saradc [3]
GPIO[8]		
GPIO[9]	EXEN	saradc [4]
GPIO[10]		saradc [5]
GPIO[11]		saradc [6]
GPIO[12]		saradc [7]
GPIO[13]		
GPIO[14]		
GPIO[15]		atest[1]
GPIO[16]		atest[0]
GPIO[17]		atest[3]
GPIO[18]		atest[2]

Application Schematic

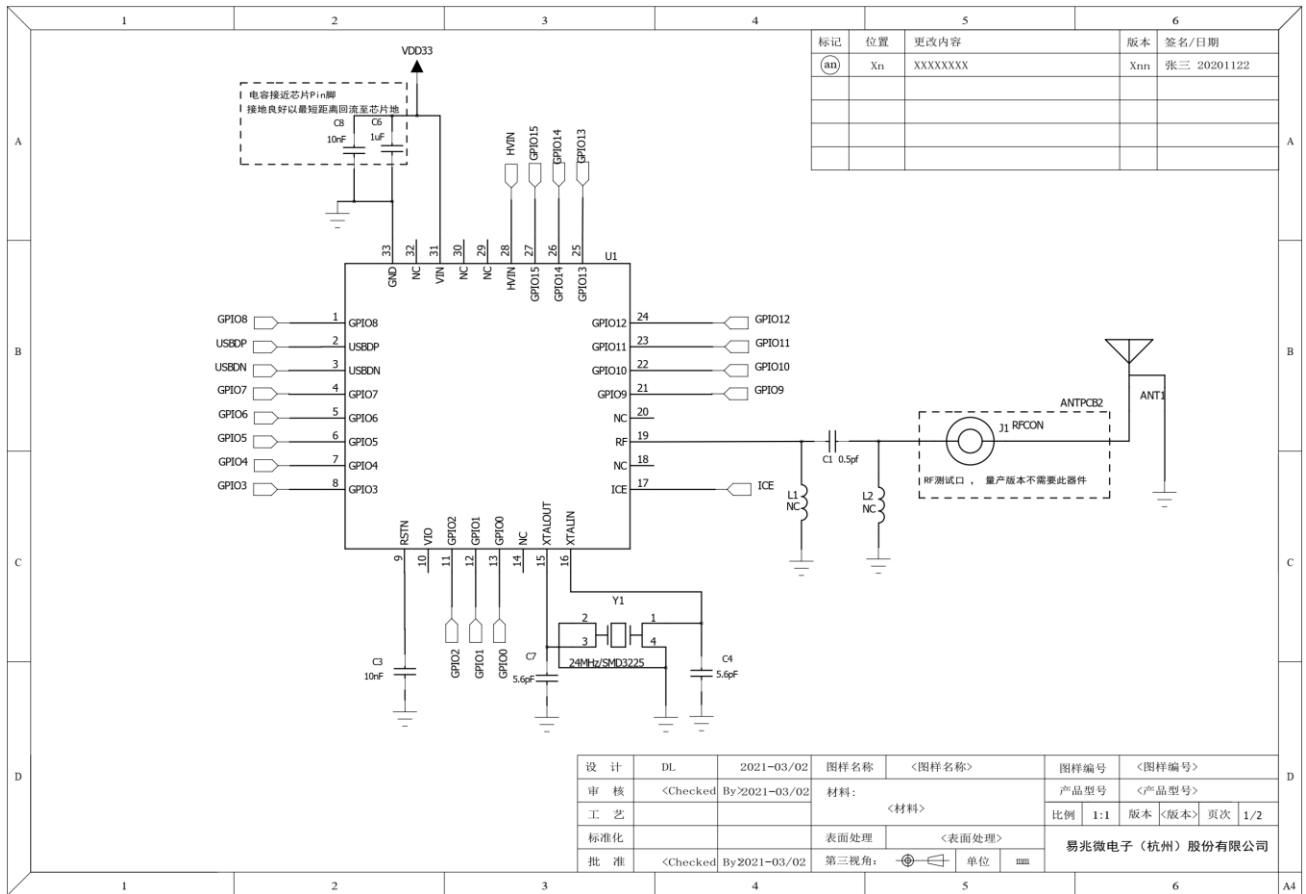


Figure 0-1 Typical application: QFN 32-pin

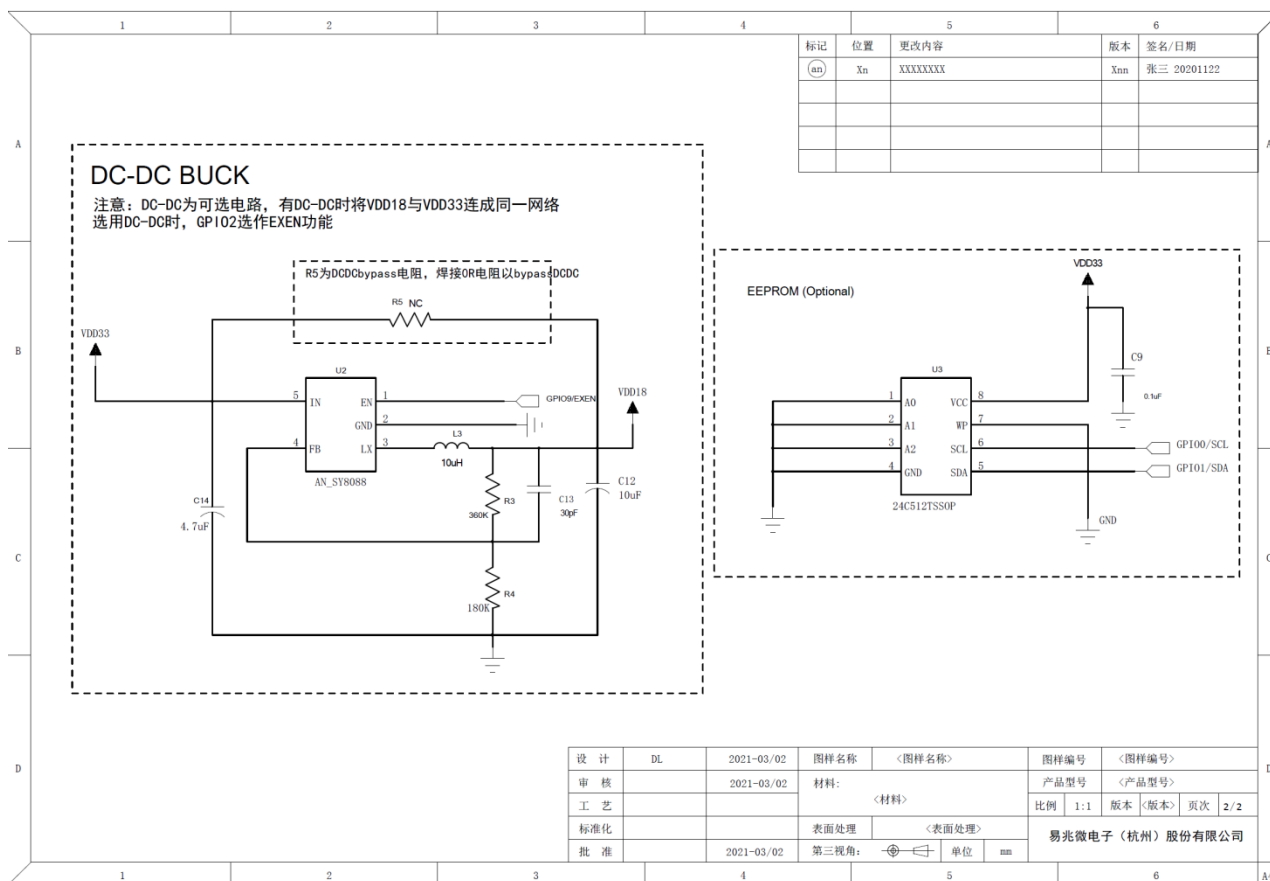


Figure 0-2 Typical application: SOP 16-pin

1 Package Information

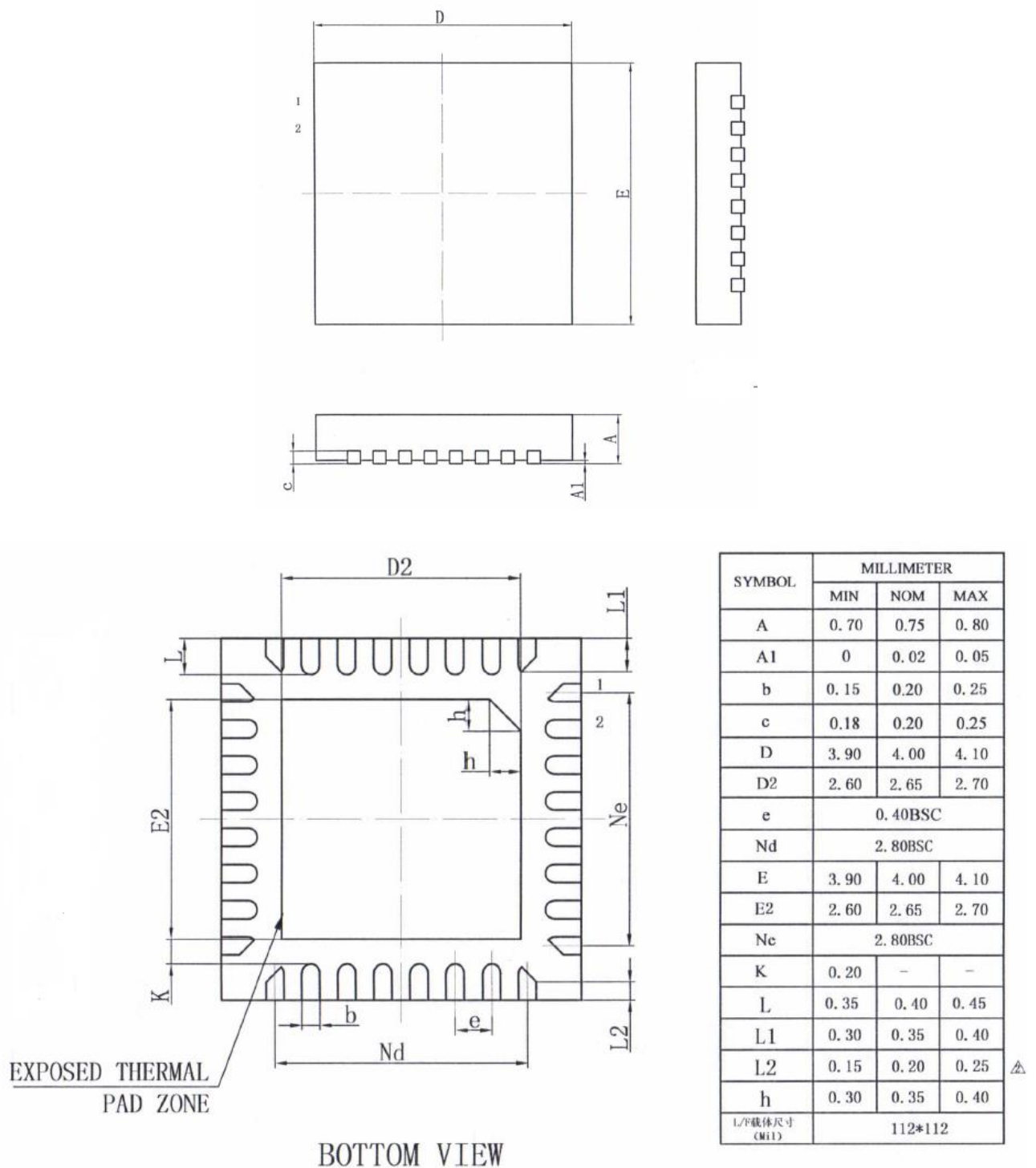


Figure 1-1 QFN32 package dimensions

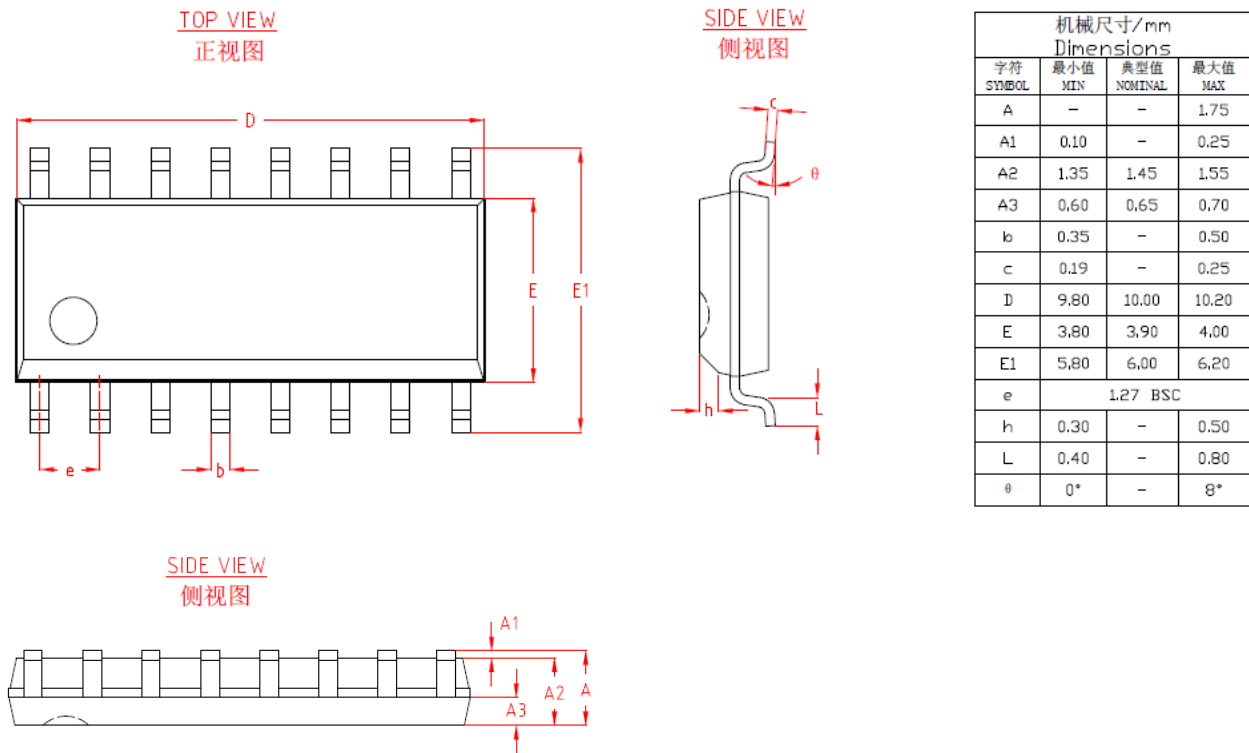


Figure 1-2 SOP16 package dimensions