

YC1306

High Performance Low Power BR/BLE 5.2 SoC

Preliminary Datasheet

General Descriptions

The YC1306 is a high performance, low power System-on-Chip (SoC) integrating a Bluetooth® 5.2 compliant 2.4-GHz transceiver, 24 MHz proprietary 32 bit MCU with a RAM of 12 KB and eFuse of 512 bits.

The YC1306 supports Bluetooth Basic Rate, Bluetooth Low Energy and Bluetooth 5.2 features including high-throughput 2 Mbps, Long Range and the Direction Finding. It can be paired through HCI interface with a more powerful MCU for applications requiring advanced wireless connectivity.

The fully-featured multiprotocol radio, +12 dBm output power, -99 dBm sensitivity and extended temperature range of -40 to 110°C makes it suitable for lighting applications.

The YC1306 features built-in USB, proprietary 32-bit MCU clocked at 24 MHz, integrated capless LDOs supporting 1.7-5.5V supply range, making it a perfect microcontroller for cost-sensitive applications such as mouse devices, toys and disposables.

Key Features

- MCU subsystems
 - 24 MHz 32-bit proprietary MCU for system control and PHY/link layer management
 - AES128 HW encryption
 - Serial wire debug
- Memories
 - 512 bit eFuse
 - 12 kB date RAM
 - 4 kB RAM supporting retention mode
- Radio transceiver
 - BR/Bluetooth 5.2/Long Range
 - +12 dBm TX power in 1dB/steps
 - -99 dBm RX sensitivity @ BLE 1 Mbps
 - -96 dBm RX sensitivity @ BLE 2 Mbps
 - Integrated balun with single-ended output and direct connection to antenna
 - 5.8 mA RX system current @ BLE 1 Mbps -99 dBm sensitivity (3V DC-DC 90% efficiency)
 - 5.2 mA RX system current @ BLE 1 Mbps -97 dBm sensitivity (3V DC-DC 90% efficiency)
 - 10.9 mA TX system current (3V DC-DC 90% efficiency, 0 dBm)
- Power management
 - Always-On (AON) supply: 1.7~ 5.5V
 - Main supply: 1.3 ~ 5.5V supporting external DCDC through a dedicated wakeup pin
 - Integrated LDOs requiring no external decoupling capacitors
 - 3.3V 40 mA capless LDO
- 1.3 μ A in sleep mode (wake on RTC, no RAM retention)
- 2 μ A in sleep mode (wake on RTC, 4 KB RAM retention)
- Clock generation
 - Dedicated PLL to support 16M/24M/26M/32M crystals
 - Crystal trimming
 - 40 MHz RC oscillator for fast wakeup
 - Low jitter low power 32 KHz RC oscillator
- 10-channel 10-bit ADC
- Digital peripherals
 - Up to 20 GPIOs w/ functions fully multiplexed
 - Two-wire master (I²C compatible) up to 600 kbps
 - 2 x UART(RTS/CTS) with HCI-H5 protocol up to 3.25 Mbps
 - 2 x SPI Master/Slave up to 24 Mbps
 - 1-axis Quadrature Decoder
 - 12 Mbps Full Speed USB 2.0
- Temperature range: -40°C to +110°C

Applications

- Mouse devices
- Toys
- Lightning applications
- Disposables
- Commercial and industrial applications requiring advanced connectivity

Key Benefits

- Best-in-class sensitivity and output power for RF-demanding applications
- BR for enhanced interoperability
- Lowest system cost for cost-oriented designs

Revision History

Version	Date	Owner	Note
0.1	3/15/2021	JH	Initial version
0.2	4/21/2021	JH	Update power consumption data
0.3	5/12/2021	Iris.li	Update Package Information

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1 Block Diagram

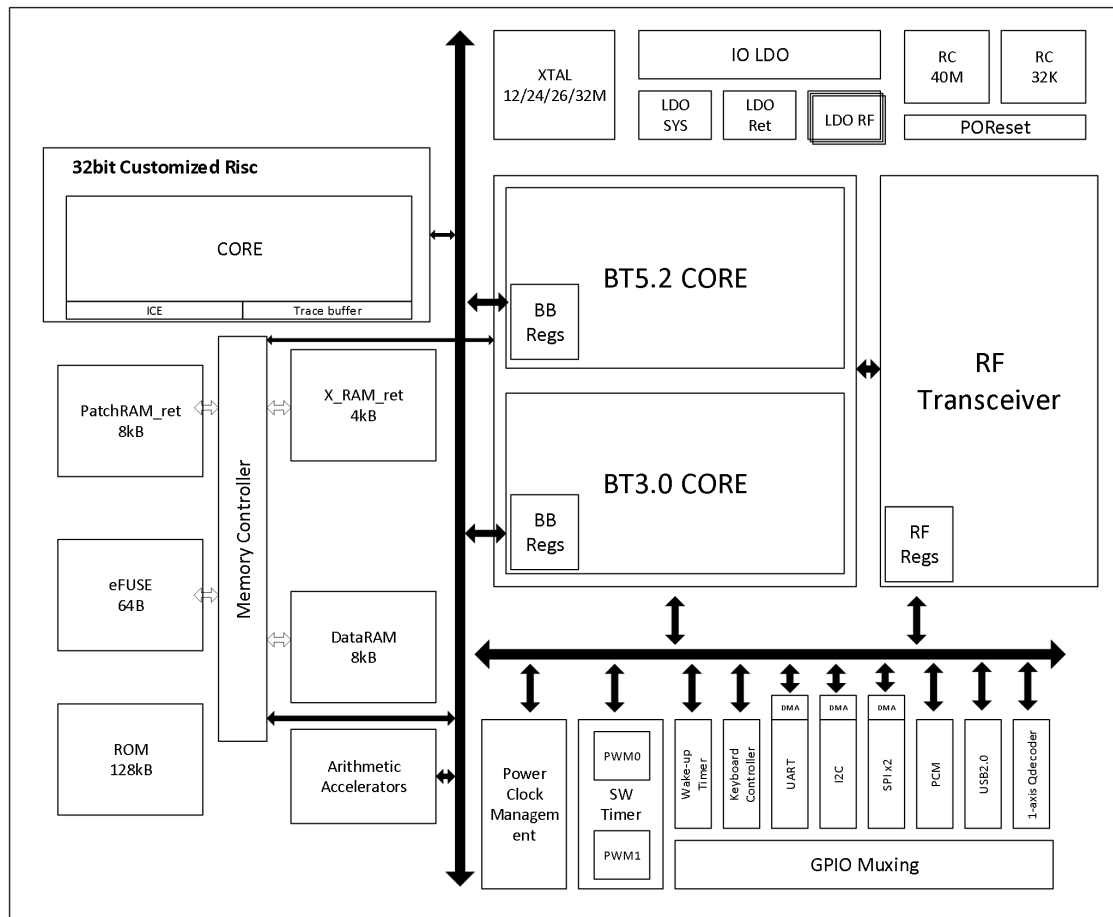


Figure 1- 1 Block diagram

2 Pinout Information

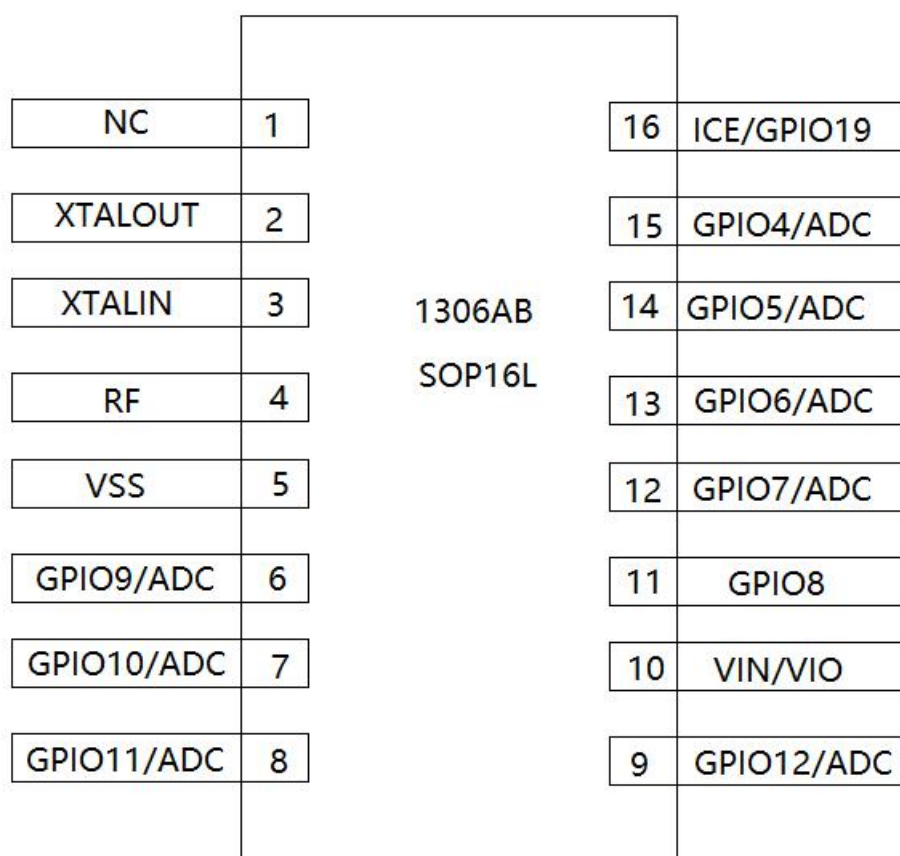


Figure 2- 2 Pinout top view (YC1306AB)

Abbreviations:

PWR: Power pin

AIO: Analog IO pin

DIO: Digital IO pin

RF: RF IO pin

Table 2- 1 Pinout Information

Pin Number	Type	Name	Description
SOP16			
1		NC	NC
2	AIO	XTALOUT	XTAL port
3	AIO	XTALIN	XTAL port, or external reference clock input
4	RF	RF	ANT port
5	GND	VSS	GND
6	DIO	GPIO9/ADC	Refer to Table 2- 2
7	DIO	GPIO10/ADC	
8	DIO	GPIO11/ADC	
9	DIO	GPIO12/ADC	
11	PWR	VIN	Main power input, 1.25~5.5V, 1μF bypass cap
12	DIO	GPIO7/ADC	Refer to Table 2- 2
13	DIO	GPIO6/ADC	
14	DIO	GPIO5/ADC	
15	DIO	GPIO4/ADC	
16	DIO	ICE/GPIO19	debug port, Tx & Rx

Note 1 : Drive capability of GPIO[19:2] is up to 100mA,GPIO[1:0] internal pullup & pulldown resistance is 1kohm.

Note 2 : GPIO[9] is by default not gpio function, and is in output high level status after por, which is used as external BUCK enable signal. GPIO[9] will restore gpio function by setting lpm_ctrl[52] to 0.

Note 3 : GPIO[9] can not used as lpm wakeup source.

Note 4 : GPIO[19] is by default in pullup status as ice function after por. GPIO[19] will restore gpio function by setting ice_mode to 0.

Table 2- 2 GPIO Multiplexing

Pin Name	boot function	function-analog
GPIO[0]		atest[5]
GPIO[1]		atest[4]
GPIO[2]		atest[7]
GPIO[3]		atest[6]
GPIO[4]		saradc [0]
GPIO[5]		saradc [1]
GPIO[6]		saradc [2]
GPIO[7]		saradc [3]
GPIO[8]		
GPIO[9]	EXEN	saradc [4]
GPIO[10]		saradc [5]
GPIO[11]		saradc [6]
GPIO[12]		saradc [7]
GPIO[13]		
GPIO[14]		

GPIO[15]		atest[1]
GPIO[16]		atest[0]
GPIO[17]		atest[3]
GPIO[18]		atest[2]
GPIO[19]	ICE	

3 Specifications

3.1 Recommended Operating Conditions

Table 3- 1 Recommended Operation Condition

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage for pin VBAT	V_{BAT}		1.55		5.5	V
Supply voltage for pin VDCDC	V_{DCDC}		1.25		5.5	V
Supply voltage for pin VIO	V_{IO}	VIO supplied by a host chip not VDD33	1.62		3.6	V
Ambient temperature	T_A		-40		110	°C

3.2 Power Consumption

Table 3- 2 Power Consumption Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sleep						
Current through pin VBAT	I_{VBAT_SLEEP}	$V_{BAT} = 3.3V$		1.3		μA
	$I_{VBAT_SLEEP_RET}$			2.0		μA
Current through pin VDCDC	I_{VDCDC_SLEEP}	$V_{DCDC} = 1.2V$		20.0		nA
RX mode 1 Mbps BLE @ -99 dBm sensitivity						
Current through pin VBAT	I_{VBAT_RX}	$V_{BAT} = 3.3V$		0.48		mA
Current through pin VLDO	I_{VLDO_RX}	$V_{DLDO} = 1.2V$	10	11.0	13	mA
Current through pin VDCDC	I_{VDCDC_RX}	$V_{LDO} = 1.2V$	5.8	6.3	7.2	mA
RX mode 1 Mbps BLE @ -97 dBm sensitivity						
Current through pin VBAT	I_{VBAT_RX}	$V_{BAT} = 3.3V$		0.48		mA
Current through pin VLDO	I_{VLDO_RX}	$V_{DLDO} = 1.2V$	9.5	10.2	12.5	mA
Current through pin VDCDC	I_{VDCDC_RX}	$V_{LDO} = 1.2V$	5.6	5.9	7	mA
TX mode 0 dBm						
Current through pin VBAT	I_{VBAT_TX}	$V_{BAT} = 3.3V$		0.48		mA
Current through pin VLDO	I_{VLDO_TX}	$V_{DCDC} = 1.2V$	17.5	18.0	19.5	mA
Current through pin	I_{VDCDC_TX}	$V_{LDO} = 1.2V$	9.2	9.5	10.2	mA

VDCDC						
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3.3 Radio

All parameters are referred to chip port and measured on the condition of VBAT = VIN = 3.3V if not stated otherwise.

Table 3- 3 Transmitter Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	f _{TX}		2325		2740	MHz
Output power	P _{out}		-20.0		15.0	dBm
Power control step	P _{step}	For part-to-part power calibrations	0.5	1.0		dB
2 nd harmonic power	P _{2harm}	0 dBm		-45.0		dBm
		4 dBm		-40.0		dBm
		12 dBm		-25.5		dBm
3 rd harmonic power	P _{3harm}	0 dBm				dBm
		4 dBm				dBm
		12 dBm				dBm
4 th harmonic power	P _{4harm}	0 dBm				dBm
		4 dBm				dBm
		12 dBm				dBm
Spurious emissions (@ 4 dBm)	P _{spur}	30 MHz to 1000 MHz		-43.7		dBm
		1 GHz to 12.75 GHz		-31.0		dBm
		47 MHz to 74 MHz		-75		dBm
		87.5 MHz to 108 MHz		-75		dBm
		174 MHz to 230 MHz		-75		dBm
		470 MHz to 862 MHz		-44.0		dBm
BDR DH1						
Average frequency deviation	Δf1 _{avg_BR}	0 dBm	156	159	162	KHz
		4 dBm	155	159.5	163	KHz
		11 dBm	153	160	169	KHz
Average frequency deviation ratio	Δf2 _{avg_BR} / Δf1 _{avg_BR}	0 dBm	0.9	0.915	0.93	
		4 dBm	0.89	0.91	0.94	
		11 dBm	0.86	0.92	0.99	
Adjacent channel power (2MHz offset)	P _{adj_BR}	0 dBm	-55	-51.3	-50	dBm
		4 dBm	-53	-48.6	-47	dBm
		11 dBm	-42	-39.7	-38	dBm
Alternate adjacent channel power (3MHz offset)	P _{aadj_BR}	0 dBm	-58	-54.3	-53	dBm
		4 dBm	-54	-52	-51	dBm
		11 dBm	-49	-43.2	-41	dBm
1 Mbps BLE						
Average frequency deviation	Δf1 _{avg_1M}	0 dBm	244	248.6	251	KHz
		4 dBm	242	248.1	253	KHz
		12 dBm	244	249.3	257	KHz
Average frequency deviation ratio	Δf2 _{avg_1M} / Δf1 _{avg_1M}	0 dBm	0.89	0.914	0.95	
		4 dBm	0.89	0.914	0.97	

		12 dBm	0.83	0.89	0.99	
Adjacent channel power (2 MHz offset)	P _{adj_1M}	0 dBm	-54	-51.4	-47	dBm
		4 dBm	-50	-47.4	-44	dBm
		12 dBm	-42	-37.4	-32	dBm
Alternate adjacent channel power (3 MHz offset)	P _{aadj_1M}	0 dBm	-57	-55.3	-53	dBm
		4 dBm	-53	-51.1	-46	dBm
		12 dBm	-46	-42.2	-39	dBm
2 Mbps BLE						
Average frequency deviation	$\Delta f_{1_avg_2M}$	0 dBm	494	497.6	502	KHz
		4 dBm	491	598.6	505	KHz
		12 dBm	470	598.3	518	KHz
Average frequency deviation ratio	$\Delta f_{2_avg_2M} / \Delta f_{1_avg_2M}$	0 dBm	0.87	0.89	0.9	
		4 dBm	0.86	0.89	0.91	
		12 dBm	0.81	0.86	0.97	
Adjacent channel power (4 MHz offset)	P _{adj_2M}	0 dBm	-59	-56.5	-54	dBm
		4 dBm	-54	-52.3	-47	dBm
		12 dBm	-47	-42.5	-34	dBm
Alternate adjacent channel power (6 MHz offset)	P _{aadj_2M}	0 dBm	-61	-58.9	-55	dBm
		4 dBm	-56	-54.3	-48	dBm
		12 dBm	-49	-44.7	-40	dBm

Table 3- 4 Receiver Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	f _{RX}		2325		2740	MHz
Out-of-band blocking	OOB	30 MHz – 2000 MHz	-30			dBm
		2003 – 2399 MHz	-35			dBm
		2484 – 2997 MHz	-35			dBm
		3000 MHz – 12.75 GHz	-30			dBm
Basic Rate						
RX sensitivity	P _{SENS_BR}	0.1 % BER	-97	-95.4	-94	dBm
C/I co-channel	C/I _{CO_BR}	0.1 % BER		7.1	11	dB
C/I 1 MHz adjacent channel	C/I _{1_1M}	0.1 % BER		-9.2	0	dB
C/I 2 MHz adjacent channel	C/I _{2_1M}	0.1 % BER		-38.1	-30	dB
C/I ≥ 3 MHz adjacent channel	C/I _{3_1M}	0.1 % BER		-44.9	-40	dB
C/I image channel	C/I _{im_1M}	0.1 % BER		-26.0	-9	dB
C/I image channel + 1MHz	C/I _{im+1_1M}	0.1 % BER		-39.5	-20	dB
Maximum input signal level	P _{IN_MAX_1M}	0.1 % BER		0.0	-20	dBm
1 Mbps BLE						
RX sensitivity	P _{SENS_1M}	0.1 % BER	-97	-99.3	- 100.5	dBm
C/I co-channel	C/I _{CO_1M}	0.1 % BER		3.8	21	dB
C/I 1 MHz adjacent channel	C/I _{1_1M}	0.1 % BER		-23.6	15	dB
C/I 2 MHz adjacent channel	C/I _{2_1M}	0.1 % BER		-26.8	-17	dB
C/I ≥ 3 MHz adjacent channel	C/I _{3_1M}	0.1 % BER		-37.9	-27	dB
C/I image channel	C/I _{im_1M}	0.1 % BER		-16.3	-9	dB
C/I image channel + 1MHz	C/I _{im+1_1M}	0.1 % BER		-19.5	-15	dB

Maximum input signal level	$P_{IN_MAX_1M}$	0.1 % BER		0.0	-10	dBm
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3.4 24 MHz Crystal Oscillator

Table 3- 5 24 MHz Crystal Oscillator Characteristic

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal frequency	f_{XTAL}		16	24	32	MHz
Crystal frequency tolerance	Δf_{XTAL}		-50		50	ppm
Load capacitance	C_{L_INN}	Programmable via registers		6	12	pF
Phase noise (referred to 24 MHz)	PN_{XTAL}	24 MHz at 100Hz offset		-115		dBc/Hz
		24 MHz at 1KHz offset		-125		dBc/Hz
		24 MHz at 10KHz offset		-135		dBc/Hz
		24 MHz at 100KHz offset		-142		dBc/Hz
		24 MHz at 1MHz offset		-146		dBc/Hz
Duty cycle	DC_{XTAL}		40.0	50.0	60.0	%
Startup time	T_{ST}	Amplitude settles to $\pm 80\%$ its normal value		1.5		mS

3.5 LDO Characteristics

Table 3- 6 LDO Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage range	V_{IN}				5.5	MHz
Output voltage	V_{OUT_SLEEP}	$I_{LOAD}=20$ mA, when input voltage below 3.3V, output equals input		3.35		V
	V_{OUT_ACTIVE}	$I_{LOAD}=100$ μ A, when input voltage below 3.3V, output equals input		3.35		V
Maximum load current	I_{LOAD}	Active mode		40		mA
Output load capacitance	C_L		0		1	μ F
Quiescent current	I_{Q_SLEEP}	doze mode		50		nA
	I_{Q_ACTIVE}	active mode		50		μ A

3.6 Reset Characteristics

Reset voltage is monitored on pin VBAT_HIGH.

Table 3- 7 Reset Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset voltage threshold	V_{POR}	rising edge	1.55	1.70	1.85	V
	V_{PDR}	falling edge	1.50	1.65	1.80	V
POR stretch time	T_{POR}			20.00		mS
PDR stretch time	T_{PDR}			20		μ S

4 Package Information

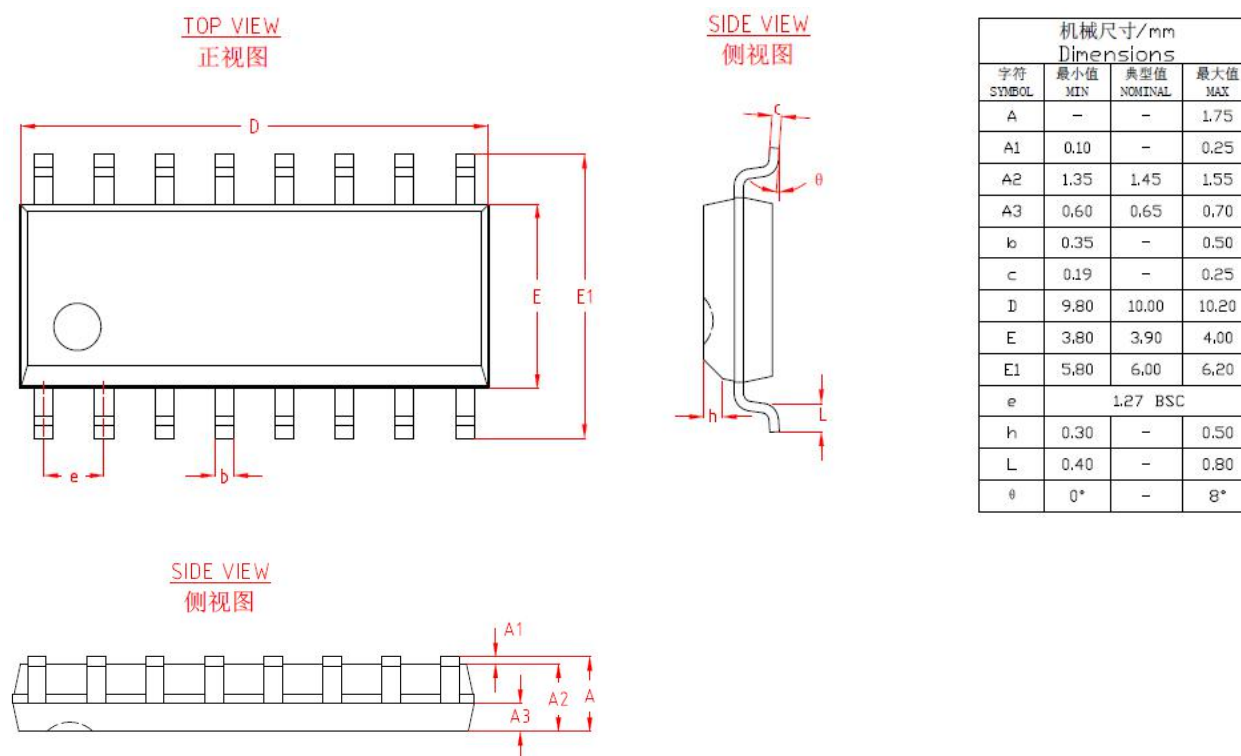


Figure 5- 2 SOP16 package dimensions