YC1168

Bluetooth 5.0 BR/EDR/BLE

Datasheet

Yichip Microelectronics

Revision History

Version	Date	Author	Description
preliminary	2019-06-18	LD	Initial version
Rev1.1	2019-06-19	GB	Added internal Flash, Modified power consumption, Added EDR for earphone use, Added current without DC/DC.

General Description

The YC1168 is a very low power, high performance and highly integrated Bluetooth 5.0 BR/EDR/BLE solution with Audio Codec, designed for operation over the 2400MHz to 2483.5Mhz ISM frequency band.

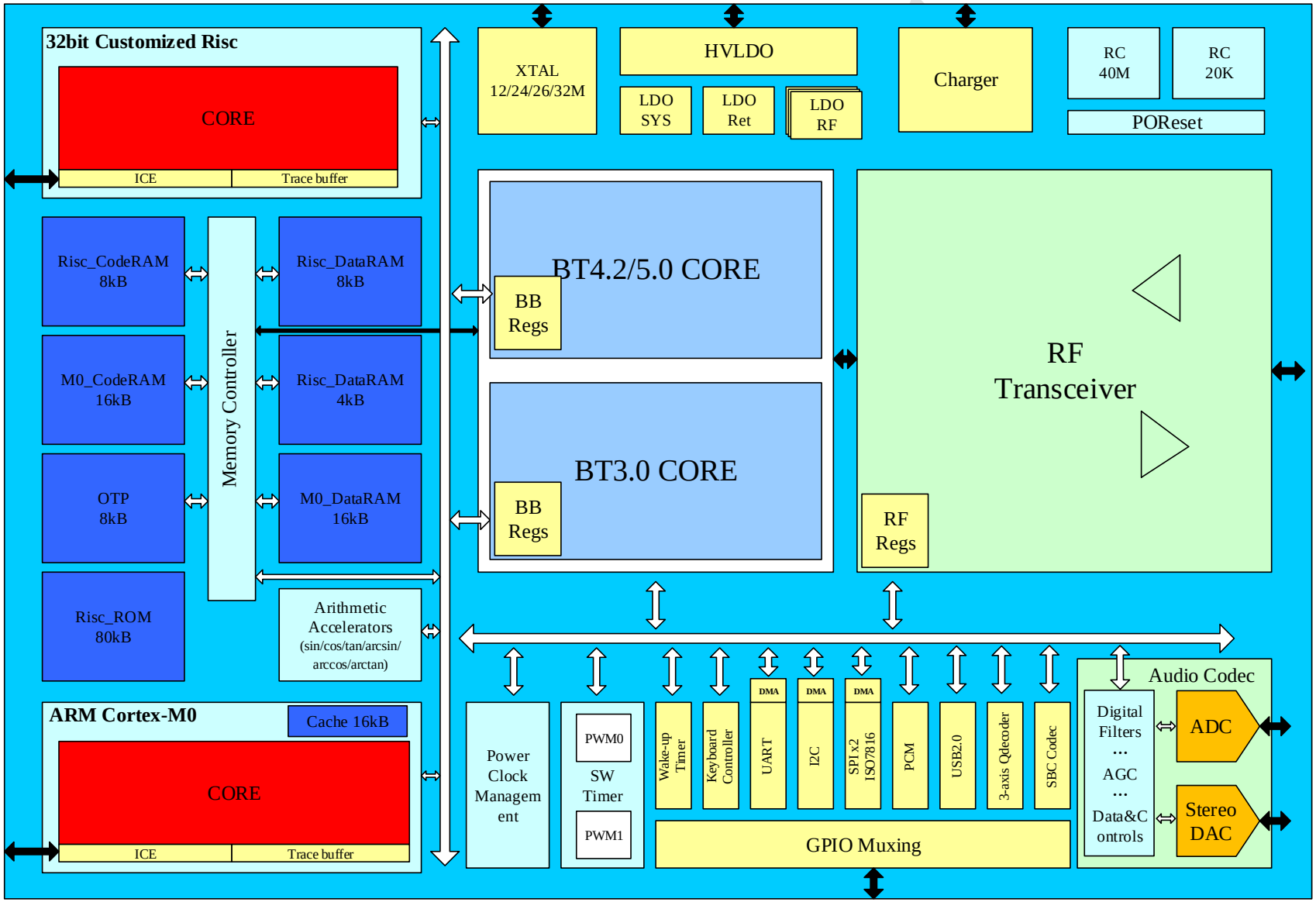
YC1168 is manufactured using advanced 55nm CMOS low leakage process, which offers highest integration, lowest power consumption, lowest leakage current and reduced BOM cost while simplifying the overall system design. Rich peripherals including an 8-channel general purpose ADC, power-on-reset (POR), Arithmetic Accelerators, 3axis Q-decoder, ISO7816, UART/SPI/I2C and 8 GPIOs, which further reduce overall system cost and size.

YC1168 operates with a power supply range from 1.8 to 5.5V and has very low power consumption in both Tx and Rx modes, enabling long lifetimes in battery-operated systems while maintaining excellent RF performance. The device can enter an ultra-low power sleep mode in which the registers and retention memory content are retained while low power Oscillator and sleep timer is ON.

Key Features

- Bluetooth 5.0 BR/EDR/BLE Proprietary double-mode RF SOC
- Very Low Power Consumption
  - 10nA shut down mode (external interrupts)
  - 800nA sleep mode (32kHz RC OSC, sleep timer and register ON)
  - 2.1uA retention mode (32kHz RC OSC, sleep timer, 2k retention memory and register ON)
  - Rx peak current w/o DCDC
    - 16mA in BLE/2.4G mode
    - 17mA in EDR mode
  - Tx peak current w/o DCDC @ -2dBm
    - 22mA in BLE/2.4G mode
    - 23mA in EDR mode
  - Rx peak current with DCDC
    - 6.75mA in BLE/2.4G mode
    - 7.25mA in EDR mode
  - Tx peak current with DCDC @ -2dBm
    - 16.5mA in BLE/2.4G mode
    - 17mA in EDR mode
  - <25uA avg, 500ms sniff hold connection
- 2.4GHz Transceiver
  - Single-end RFIO
  - -95dBm in BLE mode
  - support 250kbps, 1/2/3Mbps data rates
  - Tx Power upto +9dBm
- Audio Function
  - Mic PGA 0-18dB,3dB per step
  - 16-bits ADC
  - 2x16Bit DAC, Stereo
  - Audio SNR: ADC 88dB; DAC 92dB
- Oscillators
  - 16M/24M/32M XTAL supported (default 24M)
  - 40M RC oscillator
  - Low Jitter 20K RC oscillator
- Dual Core Digital Architecture
  - ARM Cortex-M0 Core for application
    - DataRAM 16kB+Cache 16kB
    - CPU clock speed 48Mhz
  - 32bit-Risc Core for link management
    - 80kB code ROM and 64Kbit OTP
    - 8kB patch RAM and 8kB dataRAM
    - All RAMs can be set to retention mode
- Arithmetic Accelerators *[Accuracy : (sign, 15b.16b)]*
  - sin/cos/tan/sin^{-1}/cos^{-1}/tan^{-1}/ multi/div/sqrt
- Analog Peripherals
  - 8 channel ADC with 10 bit accuracy/3Msps
- Digital Peripherals
  - Two-wire Master (I2C compatible), upto 400kbps; UART(RTS/CTS) with HCI-H5 protocol, upto 3.25Mbps; SPI Master, upto 24Mbps and internal QSPI connected 4Mbit Flash
  - ISO7816
  - AES256 HW encryption
  - LED drive capability
  - PWM
  - 20x8 key scan
  - 3 axis Q-decoder
  - USB2.0 fullspeed,4Eps

Block Diagram



Electrical Specifications

Name	Parameter (Condition)	Min	Typ	Max	Unit	Comment
Power Supplies						
HVIN	Voltage Input, typically 1uF decouple cap	3.1	4.2	5.5	V	(1)
HVOUT	Voltage Output, typically 1uF decouple cap, maximum 50mA load capability	3.1	3.3	3.4	V	
CHARGE_VAD	Voltage Input, typically 4.7uF decouple cap	4.8	5	5.5	V	
CHARGE_VBAT	Voltage Input, typically 4.7uF decouple cap	4.0	4.2	4.6	V	
IQ_HV	Quiescent Current of high voltage LDO		750		nA	
VIN	Voltage Input, typically 1uF decouple cap	1.5		3.6	V	
VINPA	Voltage Input, typically 5pF decouple cap	1.5		3.6	V	(2)
VINLPM	Voltage Input	1.8		3.6	V	(3)
VIO	Voltage Input	1.7		3.6	V	(4)
DVDD	Voltage Output, typically 1uF decouple cap	1.1	1.2	1.3	V	
VDDLPM	Voltage Output, typically 100nF decouple cap	1.1	1.2	1.3	V	
Temperature						
TEMP	Temperature	-20		+85	℃	
Digital Input Pin						
VIH	High Level	VIO-0.3		VIO+0.3	V	
VIL	Low Level	VSS		VSS+0.3	V	
Digital Onput Pin						
VOH	High Level	VIO-0.3		VIO+0.3	V	(5)
VOL	Low Level	VSS		VSS+0.3	V	
Current Consumption						
IVDD	Shut down mode, can only be waked up by wake-up pin.		10		nA	
IVDD	Retention mode (LPO, no retention RAM, POR, sleep timer, I/O interrupts ON), can be waked up by sleep timer & any GPIO		0.8		uA	(6)
IVDD	Retention mode (LPO, 2kB retention RAM, POR, sleep timer, I/O interrupts ON), can be waked up by sleep timer & any GPIO		2.1		uA	
IVDD	RX mode, BLE & 2.4G mode, 100% ON (w/o DCDC)		16		mA	(7)
IVDD	RX mode, EDR mode, 100% ON (w/o DCDC)		17		mA	
IVDD	TX mode, BLE & 2.4G mode, 100% ON (w/o DCDC)		22		mA	(8)
IVDD	TX mode, EDR mode, 100% ON (w/o		23		mA	

	DCDC)					
IVDD	RX mode, BLE & 2.4G mode, 100% ON (with ideal DCDC @3V)		6.75		mA	(7)
IVDD	RX mode, EDR mode, 100% ON (with ideal DCDC @3V)		7.25		mA	
IVDD	TX mode, BLE & 2.4G mode, 100% ON (with ideal DCDC @3V)		16.5		mA	(8)
IVDD	TX mode, EDR mode, 100% ON (with ideal DCDC @3V)		17		mA	
IVDD	Average Current, 500ms sniff, hold connection			25	uA	
Normal RF Condition						
FOP	Operating Frequency	2400		2480	MHz	
FXTAL	Crystal Frequency	12	24	32		(9)
Transmitter Characteristics						
PRF	RF output power	-20	0	9	dBm	
CD	Carrier Drift Rate		5		kHz/50 us	
PRF1	Out of band emission 2 MHz (GFSK)		-40		dBm	
PRF2	Out of band emission 3 MHz (GFSK)		-48		dBm	
BW	20dB bandwidth		0.9		MHz	
EVM	Modulation Accuracy, RMS DEVM (π/4 DQPSK)		7	20	%	
	Modulation Accuracy, RMS DEVM (8PSK)		7	13	%	
	Modulation Accuracy, 99% DEVM (π/4 DQPSK)		14	30	%	
	Modulation Accuracy, 99% DEVM (8PSK)		14	20	%	
	Modulation Accuracy, Peak DEVM (π/4 DQPSK & 8PSK)		18	35	%	
	Modulation Accuracy, Peak DEVM (8PSK)		18	25	%	
PRF1	Out of band emission 2 MHz (π/4 DQPSK & 8PSK)		-30	-20		
PRF2	Out of band emission 3 MHz (π/4 DQPSK & 8PSK)		-42	-40		
Receiver Characteristics						
	BLE					
SEN	High Gain mode, Sensitivity @0.1%		-95		dBm	
SEN	Standard Gain mode, Sensitivity @0.1%		-92		dBm	
MaxIn	Maximum Input Power		0		dBm	
C/ICO	Co-channel C/I, Basic Rate, GFSK		7		dB	
C/I1ST	ACS C/I 1MHz, Basic Rate, GFSK		5.5	7	dB	
C/I2ND	ACS C/I 2MHz, Basic Rate, GFSK		-36	-34	dB	
C/I3RD	ACS C/I 3MHz, Basic Rate, GFSK		-43		dB	

C/I1STI	ACS C/I Image channel, Basic Rate, GFSK		-34		dB	
C/I2NDI	C/I 1 MHz adjacent to image channel, Basic Rate, GFSK		-28		dB	
	BR & EDR					
SEN	Basic Rate, GFSK, BER<0.1%, Dirty Tx on		-92		dBm	
SEN	EDR, π/4 DQPSK, BER<0.01%, Dirty Tx on		-93		dBm	
SEN	EDR, 8PSK, BER<0.01%, Dirty Tx on		-83		dBm	
MaxIn	Maximum Input Power		0		dBm	
C/ICO	Co-channel C/I, EDR, π/4 DQPSK		10.5		dB	
C/I1ST	ACS C/I 1MHz, EDR, π/4 DQPSK		-8		dB	
C/I2ND	ACS C/I 2MHz, EDR, π/4 DQPSK				dB	
C/I3RD	ACS C/I 3MHz, EDR, π/4 DQPSK		-54		dB	
C/I1STI	ACS C/I Image channel, EDR, π/4 DQPSK		-27		dB	
C/I2NDI	C/I 1 MHz adjacent to image channel, EDR, π/4 DQPSK		-43		dB	
C/ICO	Co-channel C/I, EDR, 8PSK		20		dB	
C/I1ST	ACS C/I 1MHz, EDR, 8PSK		0		dB	
C/I2ND	ACS C/I 2MHz, EDR, 8PSK		-20		dB	
C/I3RD	ACS C/I 3MHz, EDR, 8PSK		-45		dB	
C/I1STI	ACS C/I Image channel, EDR, 8PSK		-18		dB	
C/I2NDI	C/I 1 MHz adjacent to image channel, EDR, 8PSK		-33		dB	

(1) HVIN & HVOUT are input & output of a high voltage LDO which is integrated in YC1168, input voltage range from 3.1~5.5V, and maximum load capability upto 50mA. Typically used in Li_BAT (3.2~4.2V) or USB_Power(4.5~5.5V) applications. If input voltage is lower than 3.6V, HVIN & HVOUT should be left unconnected and YC1168 should be powered by VIN/VINLPM/VINPA directly.

(2) If RF output power should be larger than -4dBm, VINPA should be larger than 2.5V.

(3) VINLPM should always be powered ON in all working cycles.

(4) VIO should always be powered ON in all working cycles.

(5) Drive capability of GPIO[20:30] is up to 100mA, other GPIO's drive capability is 10mA

(6) By default, 2kB retention memory is ON in retention mode. Up to 4kB retentionable X_memory available at the cost of extra 600nA retention mode current. Besides, 16kB 51-code memory is also retentionable at the cost of extra 1.6uA retention mode current.

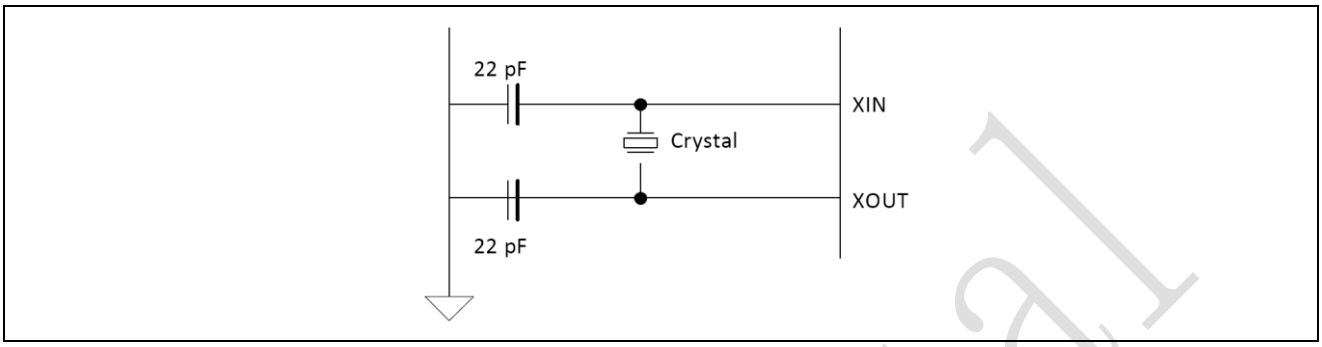
(7) Result based on standard gain mode

(8) Result based on -2dBm Pout

(9) 16M, 24M, 26M, 32M crystal supported, 24M by default

Crystal Oscilator

The crystal oscillator requires a crystal with an accuracy of ±30 ppm as defined by the Bluetooth specification. Two external load capacitors in the range of 5 pF to 30 pF are required to work with the crystal oscillator. The selection of the load capacitors is crystal dependent. The recommended crystal specification shows below.



Recommended Oscillator Configuration — 20 pF Load Crystal

Reference Crystal Electrical Specifications

Name	Parameter (Condition)	Min	Typ	Max	Unit	Comment
Frequency			24		MHz	
Oscillation mode			Fundamental			
Frequency tolerance	@25°C		±10	±30	ppm	
Tolerance stability over temp	@0°C to +70°C		±10	±30	ppm	
Load capacitance			20		pF	
Operating temperature range		-20		+70	degree	
Drive Level			100		uW	

Audio DAC

Parameter	Min	Typ	Max	Unit	Test condition
Frequency Response	20		20k	Hz	1kHz & 10kohm loading With A-Weighted Filter
Dynamic Range		90		dB	
SNR		92		dB	
THD+N		-75		dB	
Output Swing		1		Vrms	
DAC Output Power	12			mV	32ohm loading

Audio ADC

Parameter	Min	Typ	Max	Unit	Test condition
Dynamic Range		86		dB	1kHz & 10kohm loading With A-Weighted filter
SNR		88		dB	
THD+N		-75		dB	

Power consumption

W/O DC-DC	Parameter	Average Current	Unit
Sleep	/	800	nA
Sniff	500ms interval	22	uA
Discoverable	ADV interval: 640ms Scan interval: 1280ms Scan window: 11.25ms	139	uA

With DC-DC	Parameter	Average Current	Unit
Sleep	/	800	nA
Sniff	Sniff Interval:500ms	18	uA
Discoverable	ADV interval: 640ms Scan interval: 1280ms Scan window: 11.25ms	90	uA

Bluetooth Security

1. Pairing
   - Pin Code

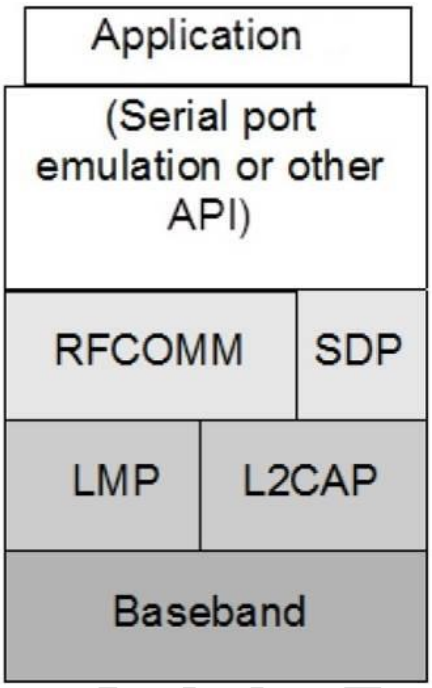
2. Security Simple Pairing
   - Just Work(No input)
   - Keyboard
   - DisplayYesNo

MFi

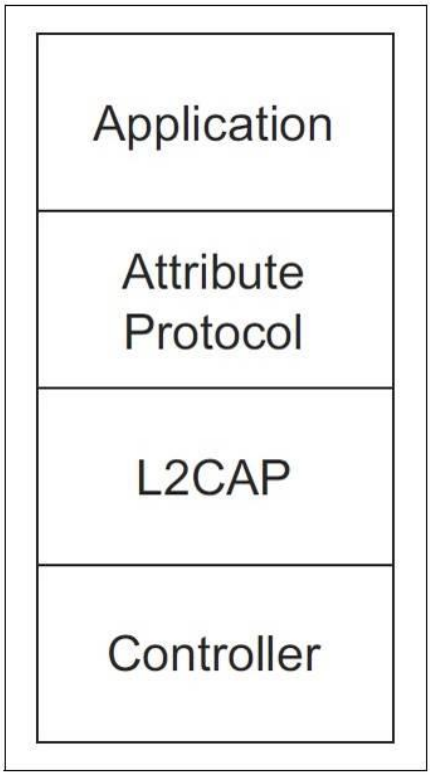
Support Apple’s MFi authentication and iAP1/iAP2 protocols.

Bluetooth Stack

1. Serial Port Profile

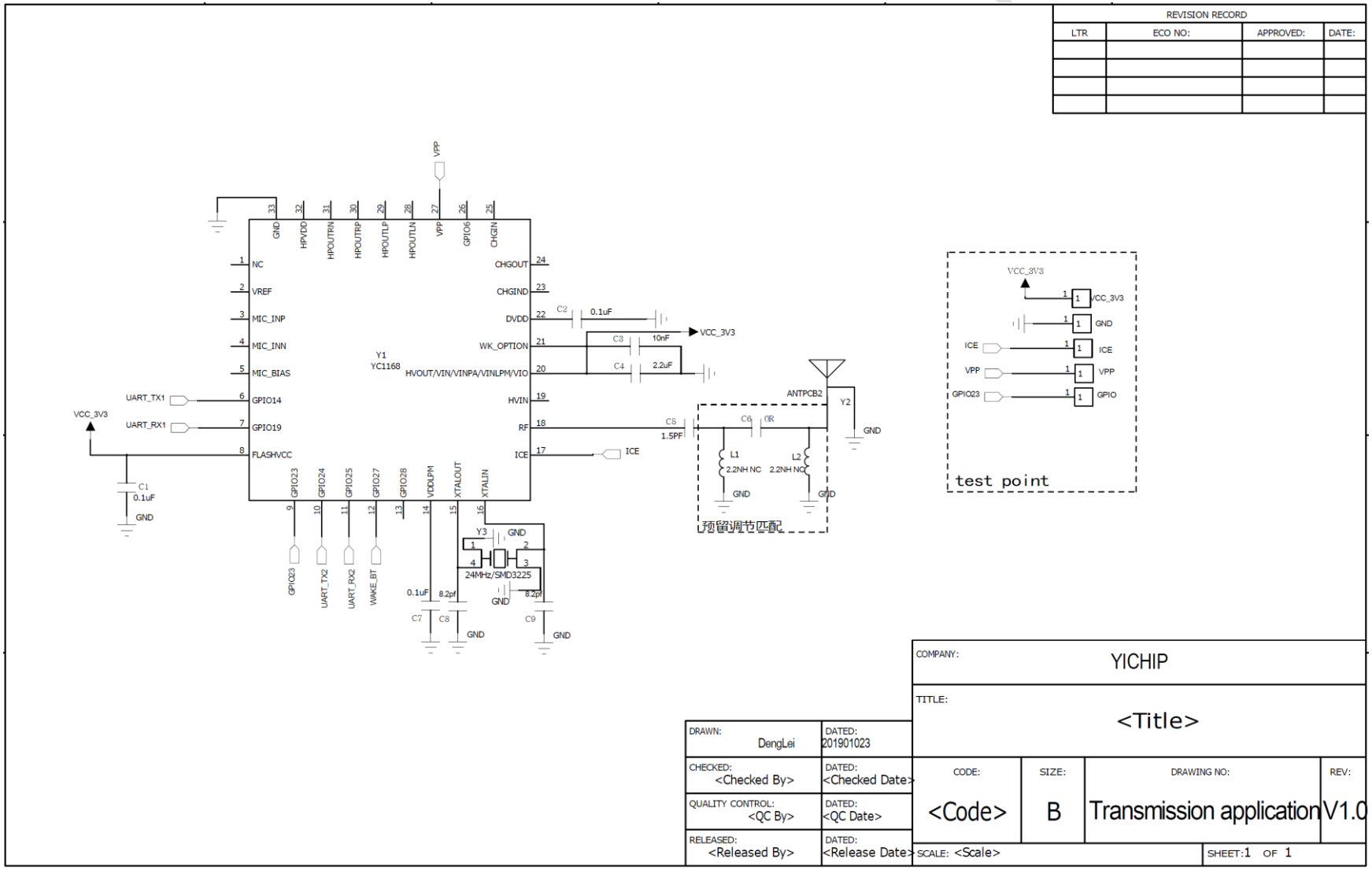


2. Generic Attribute Profile

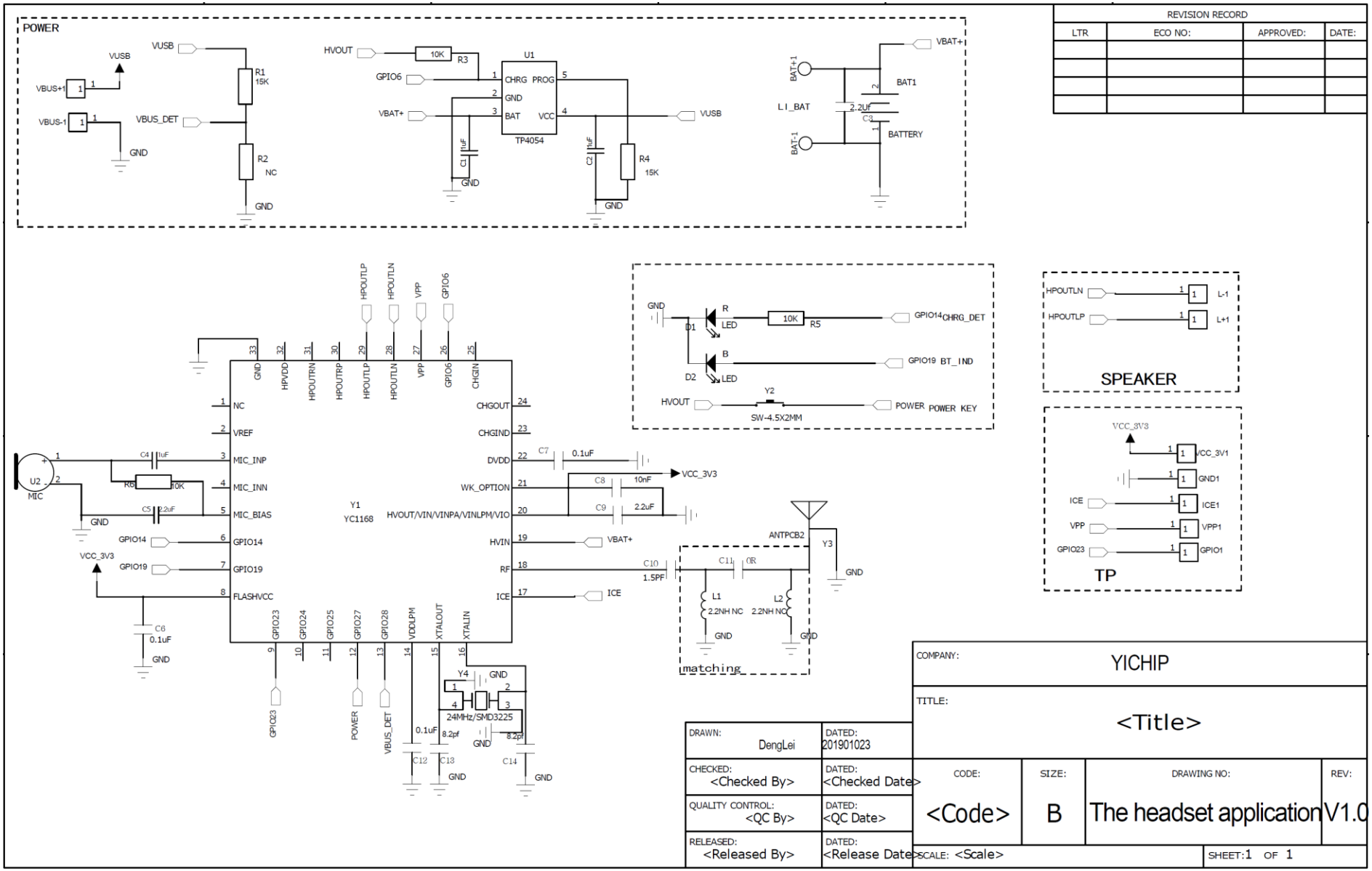


Application Schematic

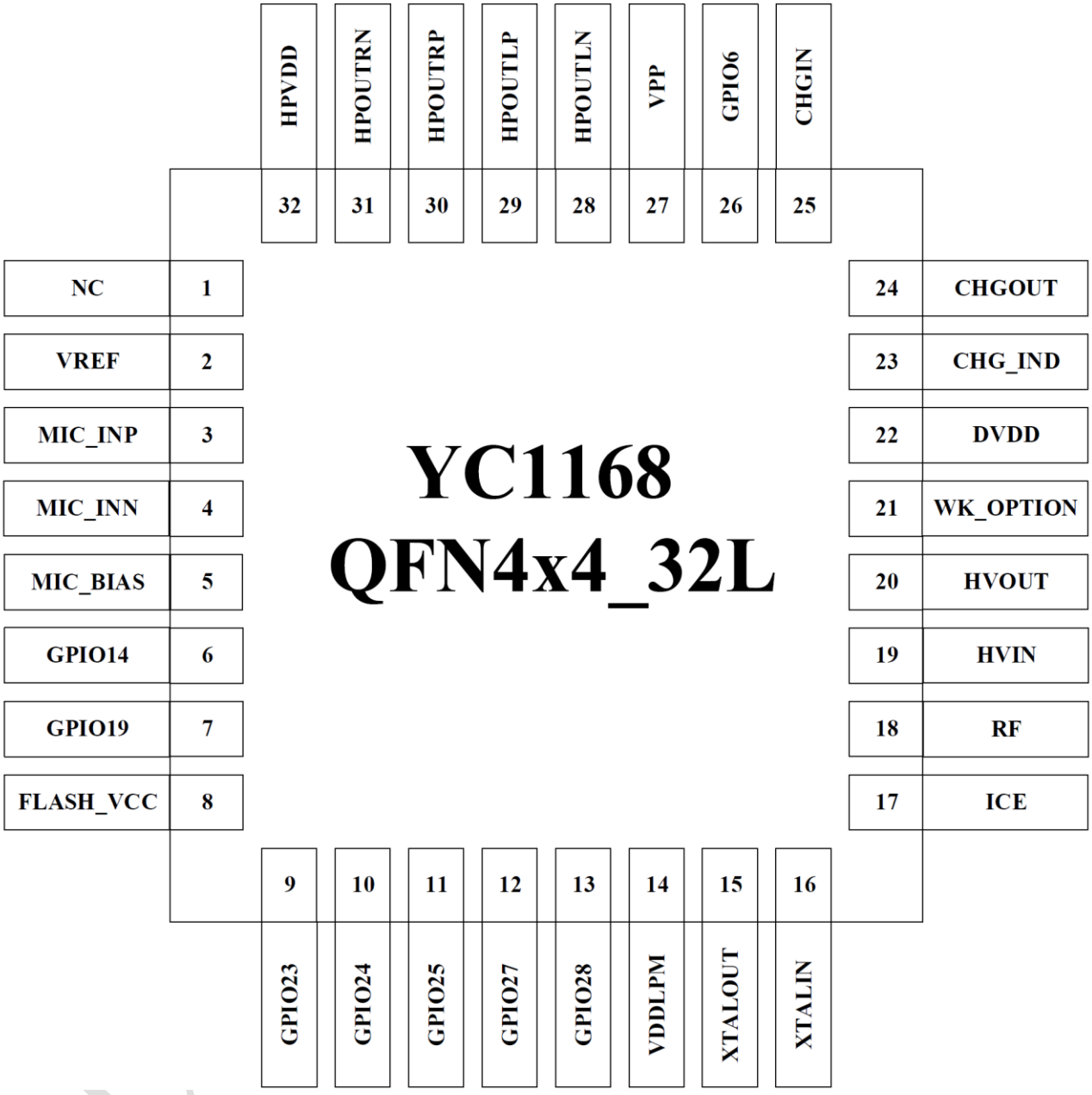
1. Transparent transmission application



2. The headset application



Package Information



4x4 32L	Pin Name	Type	Function Description
1	NC	NC	NC
2	VREFN	Power_O	Connect to an external decouple cap here 4.7uF can be optional.
3	MIC_INP	Ana_I	ADC positive input.
4	MIC_INN	Ana_I	ADC negative input.
5	MIC_BIAS	Ana_O	Power output for mic.
6	GPIO14	Dig_IO	Pls check "sheet: GPIO_Muxing"
7	GPIO19	Dig_IO	Pls check "sheet: GPIO_Muxing"
8	FLASH_VCC	Power_I	Inner flash power.
9	GPIO23	Dig_IO	Pls check "sheet: GPIO_Muxing"
10	GPIO24	Dig_IO	Pls check "sheet: GPIO_Muxing"
11	GPIO25	Dig_IO	Pls check "sheet: GPIO_Muxing"
12	GPIO27	Dig_IO	Pls check "sheet: GPIO_Muxing"
13	GPIO28	Dig_IO	Pls check "sheet: GPIO_Muxing"
14	VDDLPM	Power_O	Internal LDO output, 1.2V. Need an external bypass cap here 0.1uF.
15	XTALOUT	Ana_O	XTAL port.
16	XTALIN	Ana_I	XTAL port, or external CLK in.
17	ICE	Dig_IO	Debug port, Tx & Rx.
18	RFIO	RF Port	ANT port.
19	HVIN	Power_I	HV LDO input, 3.5~5.5V, 4.7uF bypass cap.
20	HVOUT	Power_O	HV LDO output, 3.3V. Bypass cap need here, 1uF. Max output current, 200uA@3.3V.
21	WKOPT	Dig_IO	Shutdown pin. This pin needs connect to logic high.
22	DVDD	Power_O	Internal LDO output, 1.2V. Need an external bypass cap here, 0. 1uF.
23	CHGIND	Power_O	Open-drain Charge Indication. This pin outputs a logic low when a charge cycle starts and turns to high impedance and the end-of-charge (EOC) condition is qualified. This pin is capable to sink 15mA (MIN).

24	CHGOUT	Power_O	Charger Output Pin. Connect this pin to the battery and charge current set at 150mA provide charge to 4.2V.
25	CHGIN	Power_I	Positive Input Supply Voltage provides power to the charger, Charging can range from 4.25V to 6.5V and should be bypassed with at least a 1μF capacitor.
26	GPIO6	Dig_IO	Pls check "sheet: GPIO_Muxing"
27	VPP	Power_I	OTP Program Power, 6.5V
28	HPOUTLN	Ana_O	DAC left channel negative output.
29	HPOUTLP	Ana_O	DAC left channel positive output.
30	HPOUTRP	Ana_O	DAC right channel positive output.
31	HPOUTRN	Ana_O	DAC right channel negative output.
32	HPVDD	Power_O	Need an external bypass cap here, 0.1uF.

Note: Most GPIOs are by default configured to input status after power-on reset, except for GPIO2 & GPIO24/25/26 (if applicable) which are in output status. If a GPIO is not used as well as it is not configured to output, it can be connected to GND. But GPIO2 & GPIO24/25/26 MUST NOT be connect to GND at any time.

PWM, UART, SPI and other digital peripherals can be flexibly configured to any GPIO port。

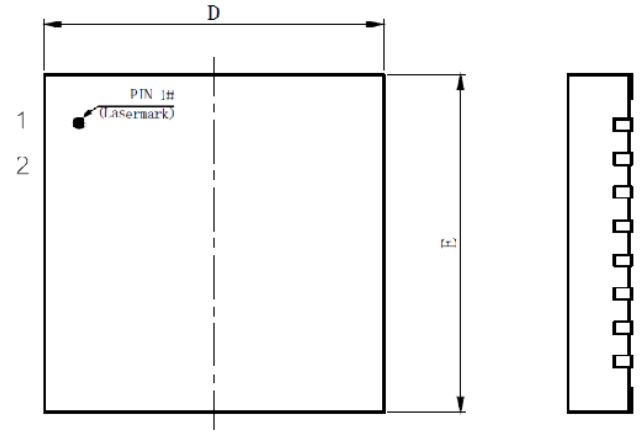
GPIO Muxing Table

GPIOs	Function1	Function2
GPIO[0]		
GPIO[1]	SPI-NCS	
GPIO[2]	SPI-IO1	
GPIO[3]	SPI-IO2	
GPIO[4]		
GPIO[5]		
GPIO[6]		
GPIO[7]		
GPIO[8]		
GPIO[9]	SPI-IO3	
GPIO[10]	SPI-SCK	
GPIO[11]	SPI-IO0	
GPIO[12]		

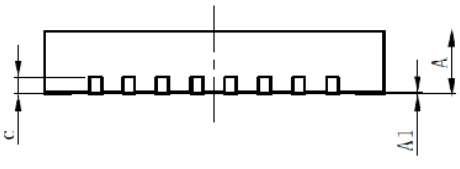
GPIO[13]		
GPIO[14]		
GPIO[15]		
GPIO[16]		
GPIO[17]		adc_channel1
GPIO[18]		adc_channel2
GPIO[19]		
GPIO[20]		adc_channel3
GPIO[21]	SDA	adc_channel4
GPIO[22]	SCL	adc_channel5
GPIO[23]		adc_channel6
GPIO[24]		adc_channel7
GPIO[25]		adc_channel8
GPIO[26]		
GPIO[27]		wakeup
GPIO[28]		wakeup
GPIO[29]		
GPIO[30]		

Note: Drive capability of GPIO[20:30] is up to 100mA, other GPIO's drive capability is 10mA;Micbias output 1.5-2.8V@3mA.

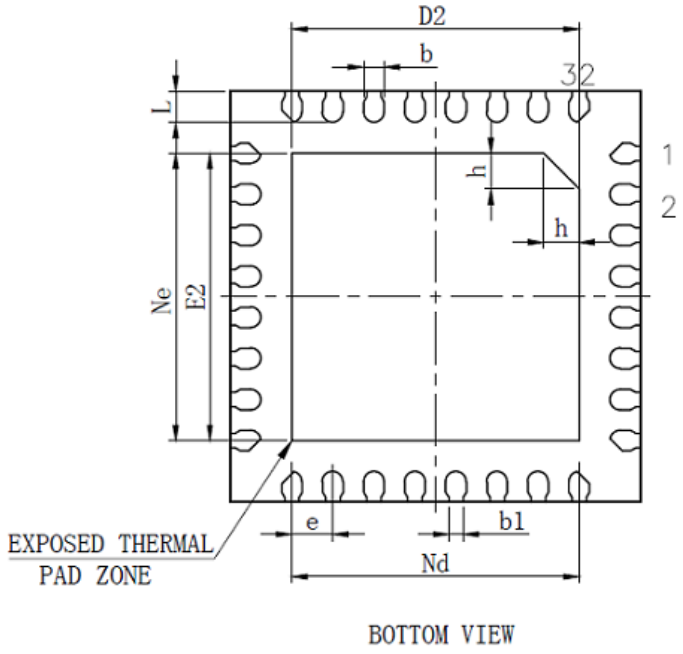
Package Physical Dimension (QFN4x4_32L)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0. 70	0.75	0. 80	
	0. 80	0.85	0. 90	⚠2
	0. 85	0.90	0. 95	⚠1
A1	0	0.02	0. 05	
b	0. 15	0.20	0. 25	
b1	0. 14REF			
c	0. 18	0.20	0. 25	
D	3. 90	4. 00	4. 10	
D2	2. 70	2. 80	2. 90	
e	0. 40BSC			
Ne	2. 80BSC			
Nd	2. 80BSC			
E	3. 90	4. 00	4. 10	
E2	2. 70	2. 80	2. 90	
L	0. 25	0.30	0. 35	
h	0. 30	0. 35	0. 40	
L/F载体尺寸	122X122			