YC1121E

Bluetooth 5.0 BR/EDR/BLE

Datasheet

Yichip Microelectronics

Revision History

Version	Date	Author	Description
preliminary	2020-1-07		Initial version
	2020-4-13		Add sch ,package and pin list
	2020-4-15	CG	Add BUCK diagram and TWS Sch

General Description

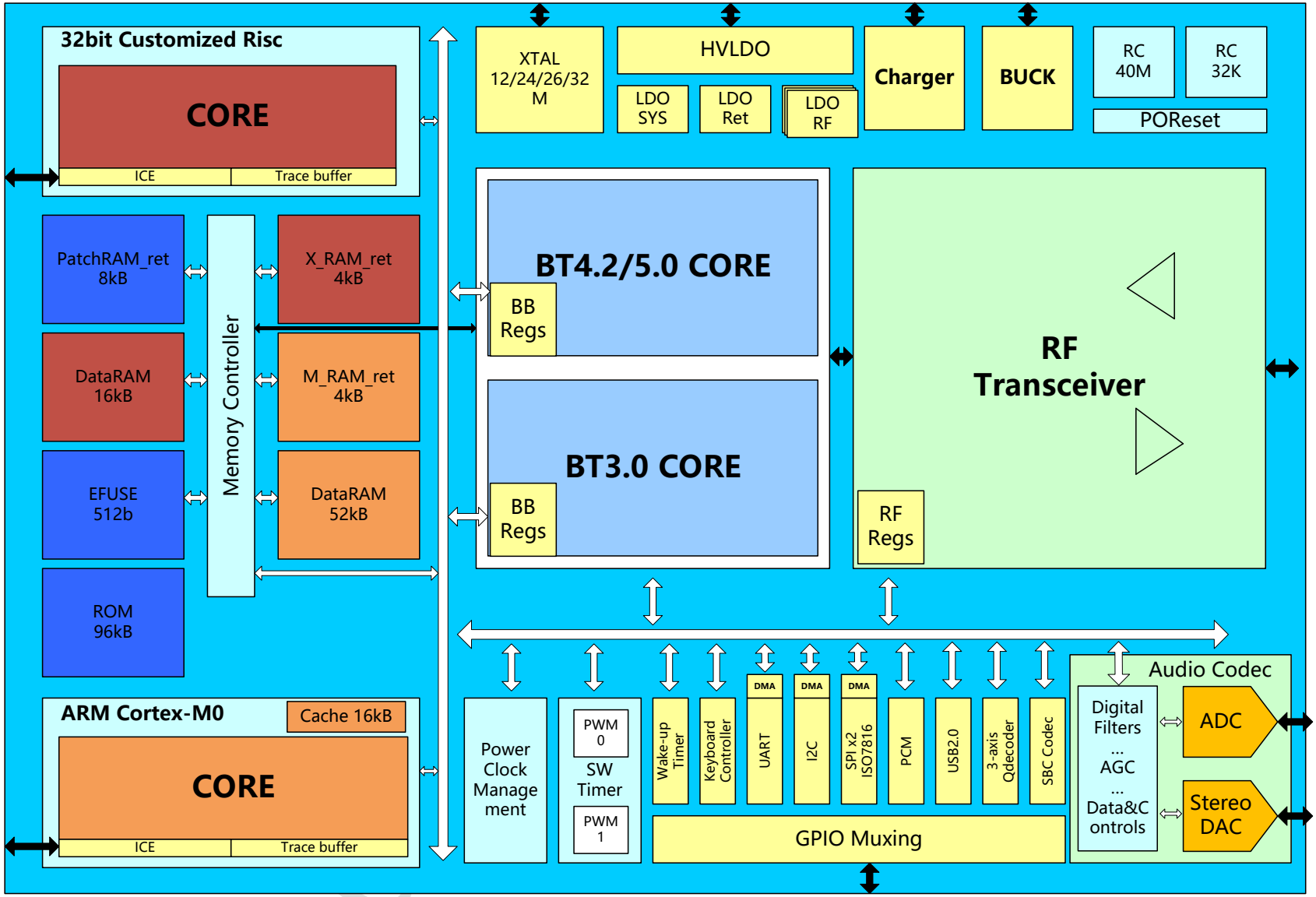
The YC1121E is a very low power, high performance and highly integrated Bluetooth 5.0 BR/EDR/BLE , designed for operation over the 2400MHz to 2483.5Mhz ISM frequency band.

YC1121E is manufactured using advanced 55nm CMOS low leakage process, which offers highest integration, lowest power consumption, lowest leakage current and reduced BOM cost while simplifying the overall system design. Rich peripherals including an 8-channel general purpose ADC, power-on-reset (POR), Arithmetic Accelerators, UART/SPI/I2C and up to 38 GPIOs, which further reduce overall system cost and size.

YC1121E operates with a power supply range from 1.8 to 5.5V and has very low power consumption in both Tx and Rx modes, enabling long lifetimes in battery-operated systems while maintaining excellent RF performance. The device can enter an ultra-low power sleep mode in which the registers and retention memory content are retained while low power Oscillator and sleep timer is ON.

Key Features

- Bluetooth 5.0 Classical/BLE Proprietary double-mode RF SOC
- Charger/Bucker integrated
- Very Low Power Consumption
  - 10nA shut down mode (external interrupts)
  - 620nA sleep mode (32kHz RC OSC, sleep timer and register ON)
  - 2uA retention mode (32kHz RC OSC, sleep timer, 2k retention memory and register ON)
  - Rx peak current w/o DCDC
    - 10mA in BLE/2.4G mode
  - Tx peak current w/o DCDC @ -2dBm
    - 18mA in BLE/2.4G mode
  - Rx peak current with DCDC
    - 6mA in BLE/2.4G mode
  - Tx peak current with DCDC @ -2dBm
    - 10mA in BLE/2.4G mode
  - <25uA avg, 500ms sniff hold connection
- 2.4GHz Transceiver
  - Single-end RFIO
  - -95dBm in BLE mode
  - support 250kbps, 1/2/3Mbps data rates
  - Tx Power up to +9dBm
- Audio function
  - Mic PGA 0-42dB,6dB per step
  - 16-bits ADC
  - 2x16Bit DAC, Stereo
  - Audio SNR: ADC 80dB; DAC 100dB
- Oscillators
  - 16M/24M/32M XTAL supported (default 24M)
  - 40M RC oscillator
  - Low Jitter 20K RC oscillator
- Dual Core Digital Architecture
  - ARM Cortex-M0 Core for application
    - Data RAM 56kB+Cache 16kB
    - CPU clock speed up to 192Mhz
  - 32bit-Risc Core for link management
    - 96kB code ROM and 512bit EFUSE
    - 8kB patch RAM and 20kB data RAM
    - 4kB RAMs can be set to retention mode
- Analog Peripherals
  - 8 channel ADC with 10 bit accuracy/3Msps
- Digital Peripherals
  - Two-wire Master (I2C compatible), up to 400kbps; UART(RTS/CTS) with HCI-H5 protocol, up to 3.25Mbps; SPI Master, up to 24Mbps, internal QSPI connect **4MB Flash**
  - Individual QSPI can connect external PSRAM
  - AES256 HW encryption
  - LED drive capability
  - PWM
  - 20x8 key scan
  - USB2.0 fullspeed,4Eps, support host mode
  - SD Card Host Controller supported


32bit Customized Risc
CORE
ICE
Trace buffer
XTAL
12/24/26/32
M
HVLDO
LDO
SYS
LDO
Ret
LDO
RF
Charger
BUCK
RC
40M
RC
32K
POReset
PatchRAM_ret
8kB
X_RAM_ret
4kB
Memory Controller
DataRAM
16kB
M_RAM_ret
4kB
EFUSE
512b
DataRAM
52kB
ROM
96kB
BT4.2/5.0 CORE
BB
Regs
BT3.0 CORE
BB
Regs
RF
Transceiver
RF
Regs
ARM Cortex-M0
Cache 16kB
CORE
ICE
Trace buffer
Power
Clock
Manage
ment
PWM
0
SW
Timer
PWM
1
Wake-up
Timer
Keyboard
Controller
DMA
UART
DMA
I2C
DMA
SPI x2
ISO7816
PCM
USB2.0
3-axis
Qdecoder
SBC Codec
GPIO Muxing
Audio Codec
Digital
Filters
...
AGC
...
Data&C
ontrols
ADC
Stereo
DAC

Electrical Specifications

Name	Parameter (Condition)	Min	Typ	Max	Unit	Comment
Power Supplies						
HVIN	Voltage Input, typically 1uF decouple cap	3.1	4.2	5.5	V	(1)
HVOUT	Voltage Output, typically 1uF decouple cap, maximum 50mA load capability	3.1	3.3	3.4	V	
CHARGE_VAD	Voltage Input, typically 4.7uF decouple cap	4.8	5	5.5	V	
CHARGE_VBAT	Voltage Input, typically 4.7uF decouple cap	4.0	4.2	4.6	V	
IQ_HV	Quiescent Current of high voltage LDO		750		nA	
VIN	Voltage Input, typically 1uF decouple cap	1.5		3.6	V	
VINPA	Voltage Input, typically 5pF decouple cap	1.5		3.6	V	(2)
VINLPM	Voltage Input	1.8		3.6	V	(3)
VIO	Voltage Input	1.7		3.6	V	(4)
DVDD	Voltage Output, typically 1uF decouple cap	1.1	1.2	1.3	V	
VDDLPM	Voltage Output, typically 100nF decouple cap	1.1	1.2	1.3	V	
Temperature						
TEMP	Temperature	-20		+85	℃	
Digital Input Pin						
VIH	High Level	VIO-0.3		VIO+0.3	V	
VIL	Low Level	VSS		VSS+0.3	V	
Digital Output Pin						
VOH	High Level	VIO-0.3		VIO+0.3	V	(5)
VOL	Low Level	VSS		VSS+0.3	V	
Current Consumption						
IVDD	Shut down mode, can only be waked up by wake-up pin.		10		nA	
IVDD	Retention mode (LPO, no retention RAM, POR, sleep timer, I/O interrupts ON), can be waked up by sleep timer & any GPIO		0.70		uA	(6)
IVDD	Retention mode (LPO, 2kB retention RAM, POR, sleep timer, I/O interrupts ON), can be waked up by sleep timer & any GPIO		1.25		uA	
IVDD	RX mode, BLE & 2.4G mode, 100% ON (with ideal DCDC @3V)		6.75		mA	(7)
IVDD	RX mode, EDR mode, 100% ON (with ideal DCDC @3V)		7.25		mA	
IVDD	TX mode, BLE & 2.4G mode, 100% ON (with ideal DCDC @3V)		16		mA	(8)
IVDD	TX mode, EDR mode, 100% ON (with ideal		17		mA	

	DCDC @3V)					
IVDD	Average Current, 500ms sniff, hold connection			25	uA	
Normal RF Condition						
FOP	Operating Frequency	2400		2480	MHz	
FXTAL	Crystal Frequency	12	24	32		(9)
Transmitter Characteristics						
PRF	RF output power	-20	0	9	dBm	
CD	Carrier Drift Rate		5		kHz/50 us	
PRF1	Out of band emission 2 MHz (GFSK)		-40		dBm	
PRF2	Out of band emission 3 MHz (GFSK)		-48		dBm	
BW	20dB bandwidth		0.9		MHz	
EVM	Modulation Accuracy, RMS DEVM (π/4 DQPSK)		7	20	%	
	Modulation Accuracy, RMS DEVM (8PSK)		7	13	%	
	Modulation Accuracy, 99% DEVM (π/4 DQPSK)		14	30	%	
	Modulation Accuracy, 99% DEVM (8PSK)		14	20	%	
	Modulation Accuracy, Peak DEVM (π/4 DQPSK & 8PSK)		18	35	%	
	Modulation Accuracy, Peak DEVM (8PSK)		18	25	%	
PRF1	Out of band emission 2 MHz (π/4 DQPSK & 8PSK)		-30	-20		
PRF2	Out of band emission 3 MHz (π/4 DQPSK & 8PSK)		-42	-40		
Receiver Characteristics						
	BT4.0 (BLE)					
SEN	High Gain mode, Sensitivity @0.1%		-95		dBm	
SEN	Standard Gain mode, Sensitivity @0.1%		-92		dBm	
Max In	Maximum Input Power		0		dBm	
C/ICO	Co-channel C/I, Basic Rate, GFSK		7		dB	
C/I1ST	ACS C/I 1MHz, Basic Rate, GFSK		5.5	7	dB	
C/I2ND	ACS C/I 2MHz, Basic Rate, GFSK		-36	-34	dB	
C/I3RD	ACS C/I 3MHz, Basic Rate, GFSK		-43		dB	
C/I1STI	ACS C/I Image channel, Basic Rate, GFSK		-34		dB	
C/I2NDI	C/I 1 MHz adjacent to image channel, Basic Rate, GFSK		-28		dB	
	BT3.0 (BR & EDR)					
SEN	Basic Rate, GFSK, BER<0.1%, Dirty Tx on		-92		dBm	
SEN	EDR, π/4 DQPSK, BER<0.01%, Dirty Tx on		-93		dBm	
SEN	EDR, 8PSK, BER<0.01%, Dirty Tx on		-83		dBm	

MaxIn	Maximum Input Power		0		dBm	
C/ICO	Co-channel C/I, EDR, π/4 DQPSK		10.5		dB	
C/I1ST	ACS C/I 1MHz, EDR, π/4 DQPSK		-8		dB	
C/I2ND	ACS C/I 2MHz, EDR, π/4 DQPSK				dB	
C/I3RD	ACS C/I 3MHz, EDR, π/4 DQPSK		-54		dB	
C/I1STI	ACS C/I Image channel, EDR, π/4 DQPSK		-27		dB	
C/I2NDI	C/I 1 MHz adjacent to image channel, EDR, π/4 DQPSK		-43		dB	
C/ICO	Co-channel C/I, EDR, 8PSK		20		dB	
C/I1ST	ACS C/I 1MHz, EDR, 8PSK		0		dB	
C/I2ND	ACS C/I 2MHz, EDR, 8PSK		-20		dB	
C/I3RD	ACS C/I 3MHz, EDR, 8PSK		-45		dB	
C/I1STI	ACS C/I Image channel, EDR, 8PSK		-18		dB	
C/I2NDI	C/I 1 MHz adjacent to image channel, EDR, 8PSK		-33		dB	

(1) HVIN & HVOUT are input & output of a high voltage LDO which is integrated in YC1121, input voltage range from 3.1~5.5V, and maximum load capability upto 50mA. Typically used in Li_BAT (3.2~4.2V) or USB_Power(4.5~5.5V) applications. If input voltage is lower than 3.6V, HVIN & HVOUT should be left unconnected and YC1121 should be powered by VIN/VINLPM/VINPA directly.

(2) If RF output power should be larger than -4dBm, VINPA should be larger than 2.5V.

(3) VINLPM should always be powered ON in all working cycles.

(4) VIO should always be powered ON in all working cycles.

(5) Drive capability of GPIO[20:30] is up to 100mA, other GPIO's drive capability is 10mA

(6) By default, 2kB retention memory is ON in retention mode. Up to 4kB retentionable X_memory available at the cost of extra 600nA retention mode current. Besides, 16kB 51-code memory is also retentionable at the cost of extra 1.6uA retention mode current.

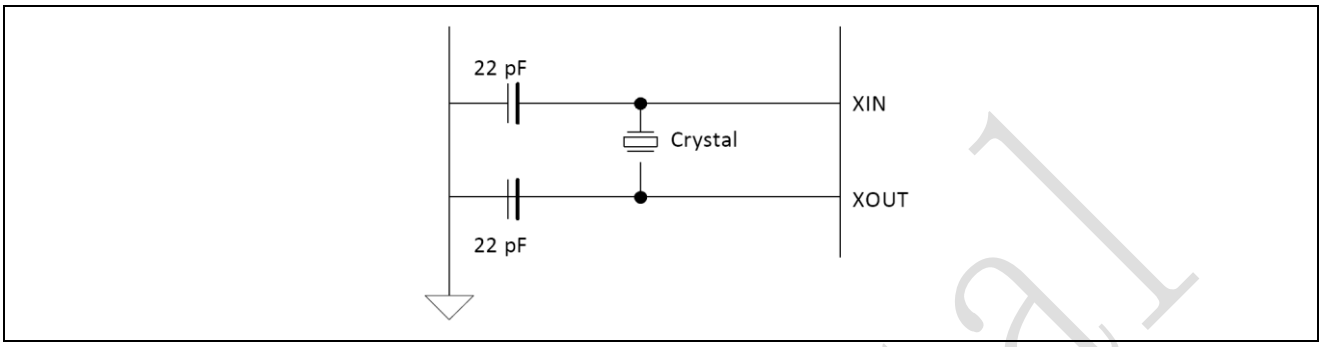
(7) Result based on standard gain mode

(8) Result based on -2dBm Pout

(9) 16M, 24M, 26M, 32M crystal supported, 24M by default

Crystal Oscillator

The crystal oscillator requires a crystal with an accuracy of ±30 ppm as defined by the Bluetooth specification. Two external load capacitors in the range of 5 pF to 30 pF are required to work with the crystal oscillator. The selection of the load capacitors is crystal dependent. The recommended crystal specification shows below.



Recommended Oscillator Configuration — 20 pF Load Crystal

Reference Crystal Electrical Specifications

Name	Parameter (Condition)	Min	Typ	Max	Unit	Comment
Frequency			24		MHz	
Oscillation mode			Fundamental			
Frequency tolerance	@25℃		±10	±30	ppm	
Tolerance stability over temp	@0℃ to +70℃		±10	±30	ppm	
Load capacitance			20		pF	
Operating temperature range		-20		+70	degree	
Drive Level			100		uW	

Audio DAC

Parameter	Min	Typ	Max	Unit	Test condition
Frequency Response	20		20k	Hz	1kHz/0dB 10kohm loading With A-Weighted Filter
THD+N		-80		dB	
S/N		98		dB	
Output Swing		1		Vrms	
Dynamic Range		90		dB	1kHz/-60dB 10kohm loading With A-Weighted filter
DAC Output Power		31		mW	32ohm loading

Audio ADC

Parameter	Min	Typ	Max	Unit	Test condition
Dynamic Range		80		dB	1kHz/-60dB
S/N		75		dB	10kohm loading
THD+N		-65		dB	With A-Weighted filter

Power consumption

W/O DC-DC	Parameter	Average Current	Unit
Sleep	/	700	nA
Sniff	500ms interval	21.99	uA
Discoverable	ADV interval: 640ms Scan interval: 1280ms Scan window: 11.25ms	138.66	uA

With DC-DC	Parameter	Average Current	Unit
Sleep	/	700	nA
Sniff	Sniff Interval:500ms	17.92	uA
Discoverable	ADV interval: 640ms Scan interval: 1280ms Scan window: 11.25ms	89.5	uA

Bluetooth Security

1. Pairing
   - Pin Code

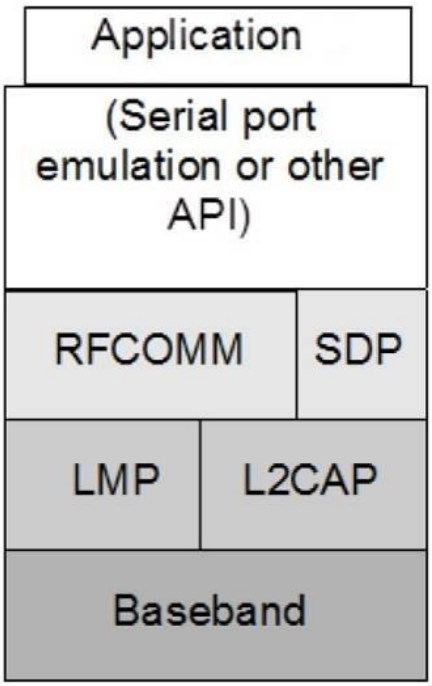
2. Security Simple Pairing
   - Just Work(No input)
   - Keyboard
   - DisplayYesNo

MFi

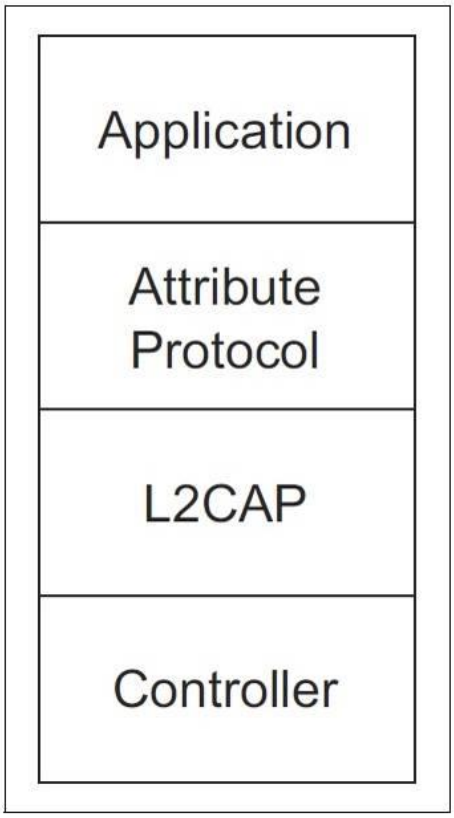
Support Apple’s MFi authentication and iAP1/iAP2 protocols.

Bluetooth Stack

1. Serial Port Profile

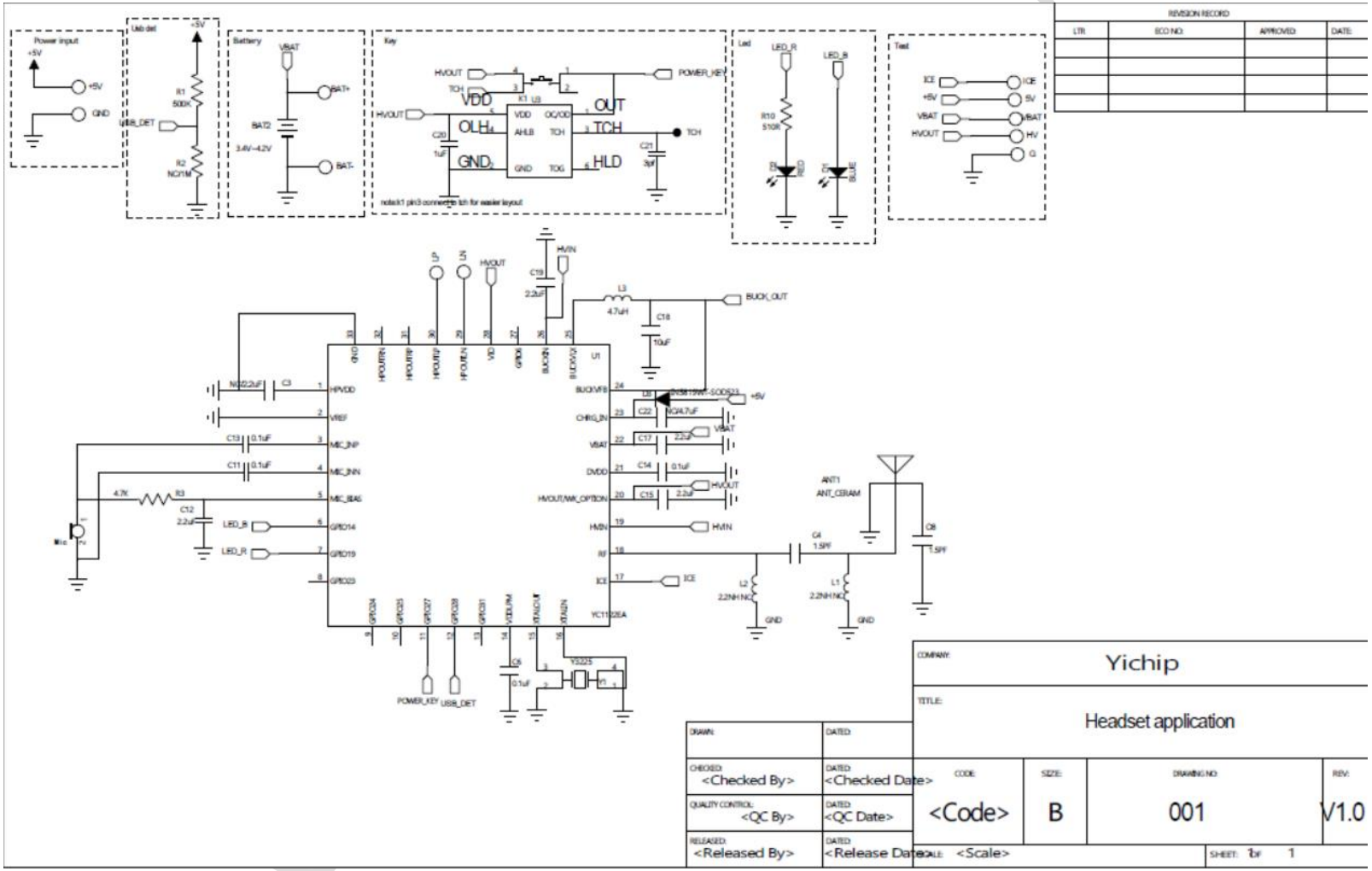


2. Generic Attribute Profile

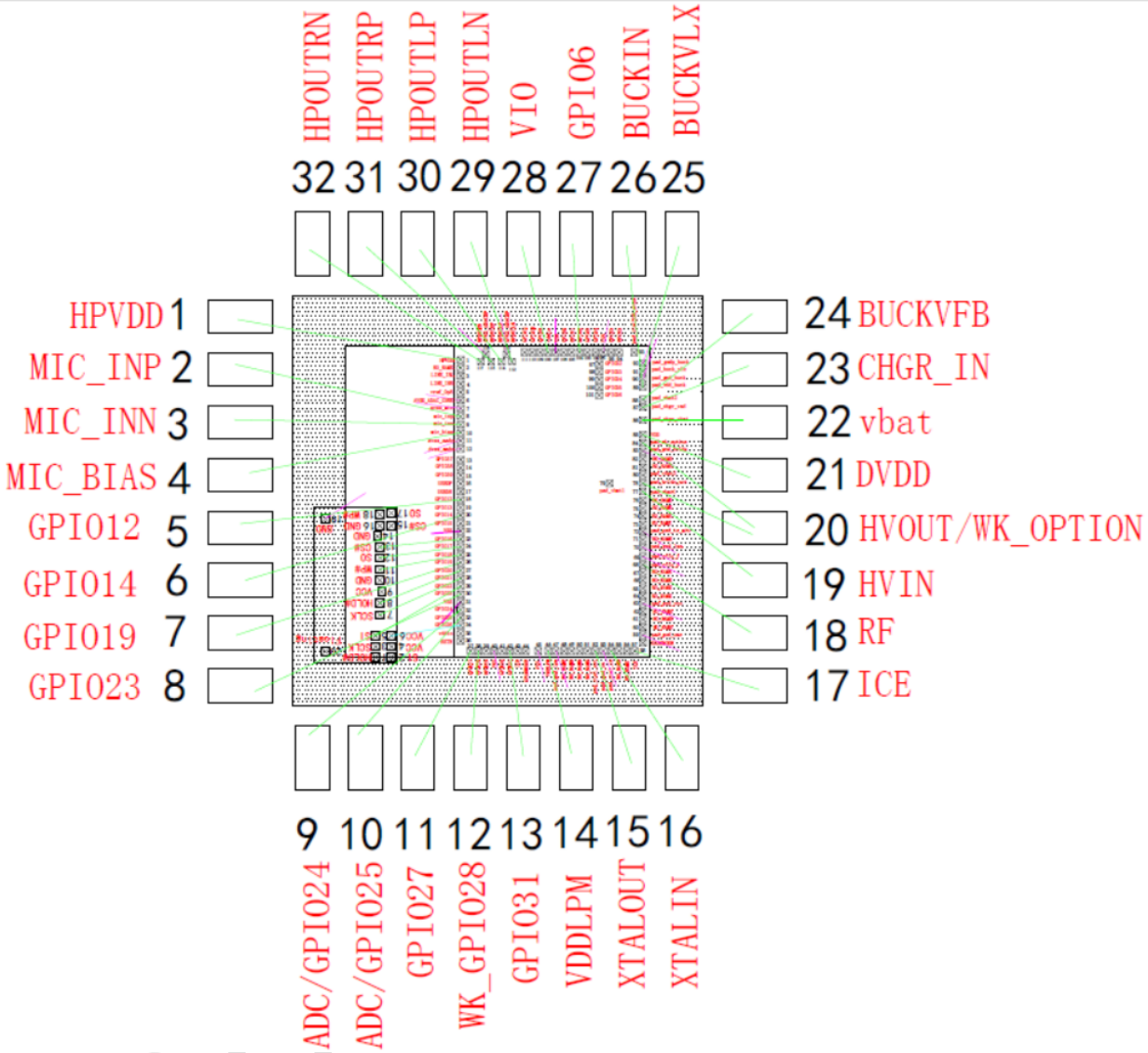


Application Schematic

1.The headset application



Package Information



7x7 68L	4x4 32L	Pin Name	Type	Function Description
1		NC		
2	1	HPVDD	Power_O	Connect an external decouple cap here 4.7uF,can optional.
3		LINE_INL	Ana_I	Line left input
4		LINE_INR	Ana_I	Line right input
5	2	VREF_0P8	Power_O	Connect an external decouple cap here 4.7uF,can optional.
6	3	MIC_INP	Ana_I	ADC positive input.
7	4	MIC_INN	Ana_I	ADC negative input.
8	5	MIC_BIAS	Ana_O	Power output for mic,1.5-2.8v,need 1uF bypass cap.
9		GPIO37	Dig_IO	pls check "sheet: GPIO_Muxing"
10		GPIO38	Dig_IO	pls check "sheet: GPIO_Muxing"
11		GPIO39	Dig_IO	pls check "sheet: GPIO_Muxing"

12		USB_DP	Dig_IO	USB port.
13		USB_DN	Dig_IO	USB port.
14		GPIO12	Dig_IO	pls check "sheet: GPIO_Muxing"
15		GPIO13	Dig_IO	pls check "sheet: GPIO_Muxing"
16	6	GPIO14	Dig_IO	pls check "sheet: GPIO_Muxing"
17		GPIO15	Dig_IO	pls check "sheet: GPIO_Muxing"
18	7	GPIO19	Dig_IO	pls check "sheet: GPIO_Muxing"
19		FLASH-VCC	Power_I	Internal FLASH power supply ,need 0.1uF bypass cap.
20	8	GPIO23	Dig_IO	pls check "sheet: GPIO_Muxing"
21	9	GPIO24	Dig_IO	pls check "sheet: GPIO_Muxing"
22	10	GPIO25	Dig_IO	pls check "sheet: GPIO_Muxing"
23		GPIO26	Dig_IO	pls check "sheet: GPIO_Muxing"
24	28	VDDIO	Power_O	GPIO power supply,need an external bypass cap here 10nF.
25		RSTN	Dig_IO	Global reset, active low. OR gated with internal POR. If not needed an external bypass cap here 10nF.
26	11	GPIO27	Dig_IO	pls check "sheet: GPIO_Muxing"
27	12	GPIO28	Dig_IO	pls check "sheet: GPIO_Muxing"
28		GPIO29	Dig_IO	pls check "sheet: GPIO_Muxing"
29		GPIO30	Dig_IO	pls check "sheet: GPIO_Muxing"
30	13	GPIO31	Dig_IO	pls check "sheet: GPIO_Muxing"
31	14	VDDLPM	Power_O	internal LDO output, 1.2V. Need an external bypass cap here 0.1uF.
32	15	XTALOUT	Ana_O	XTAL port.
33	16	XTALIN	Ana_I	XTAL port, or external CLK in.
34	17	ICE	Dig_IO	debug port, Tx & Rx.
35		SCANMODE	Dig_I	SCAN Test enable pin.
36	18	RFIO	RF Port	ANT port.
37	19	HVIN	Power_I	HVLDO input, 3.6~5.5V, 2.2uF bypass cap.
38	20	HVOUT	Power_O	HVLDO output, 3.3V. Bypass cap need here 2.2uF,max output current 150mA@3.3V.
39		NC		
40	20	WKOPT	Dig_IO	Shutdown pin.This pin need connect to logic high.
41	21	DVDD	Power_O	internal LDO output, 1.2V. Need an external bypass cap here0. 1uF.
42	22	CHGOUT	Power_O	Charger Output Pin. Connect this pin to the battery and charge current be set at 40mA .provides charge to 4.2V.
43	23	CHGIN	Power_I	Positive Input Supply Voltage. provides power to the charger,Chrgin can range from 4.25V to 5.5V .need bypassed with at least a 1μF capacitor and series a schottky diode.
44	24	VIN/BUCKOUT	Power_O	Buckout pin output 1.8~3.6V internal connect to VIN, 10uF bypass cap.
45	26	BUCKIN	Power_I	Buck input 3.6~4.2V,10uF bypass cap.
46	25	BUCKVLX	Power_adj	Need an external bypass inductor here 10uH connect to buckout.
47		NC		
48		NC		

49		GPIO36	Dig_IO	pls check "sheet: GPIO_Muxing"
50		GPIO35	Dig_IO	pls check "sheet: GPIO_Muxing"
51		GPIO34	Dig_IO	pls check "sheet: GPIO_Muxing"
52		NC		
53		GPIO2	Dig_IO	pls check "sheet: GPIO_Muxing"
54		GPIO3	Dig_IO	pls check "sheet: GPIO_Muxing"
55		GPIO33	Dig_IO	pls check "sheet: GPIO_Muxing"
56		GPIO32	Dig_IO	pls check "sheet: GPIO_Muxing"
57		GPIO4	Dig_IO	pls check "sheet: GPIO_Muxing"
58		GPIO5	Dig_IO	pls check "sheet: GPIO_Muxing"
59	27	GPIO6	Dig_IO	pls check "sheet: GPIO_Muxing"
60		GPIO7	Dig_IO	pls check "sheet: GPIO_Muxing"
61		GPIO8	Dig_IO	pls check "sheet: GPIO_Muxing"
62		GPIO9	Dig_IO	pls check "sheet: GPIO_Muxing"
63		GPIO10	Dig_IO	pls check "sheet: GPIO_Muxing"
64		GPIO11	Dig_IO	pls check "sheet: GPIO_Muxing"
65	29	HPOUTLN	Ana_O	DAC left channel negative output.
66	30	HPOUTLP	Ana_O	DAC left channel positive output.
67	31	HPOUTRP	Ana_O	DAC right channel positive output.
68	32	HPOUTRN	Ana_O	DAC right channel negative output.

Note: All GPIOs are by default configured to input status after power-on reset, and ICE are by default configured to high level by pull up. If a GPIO is not used as well as it is not configured to output, it can be connected to GND.

PWM, UART, SPI and other digital peripherals can be flexibly configured to any GPIO port。

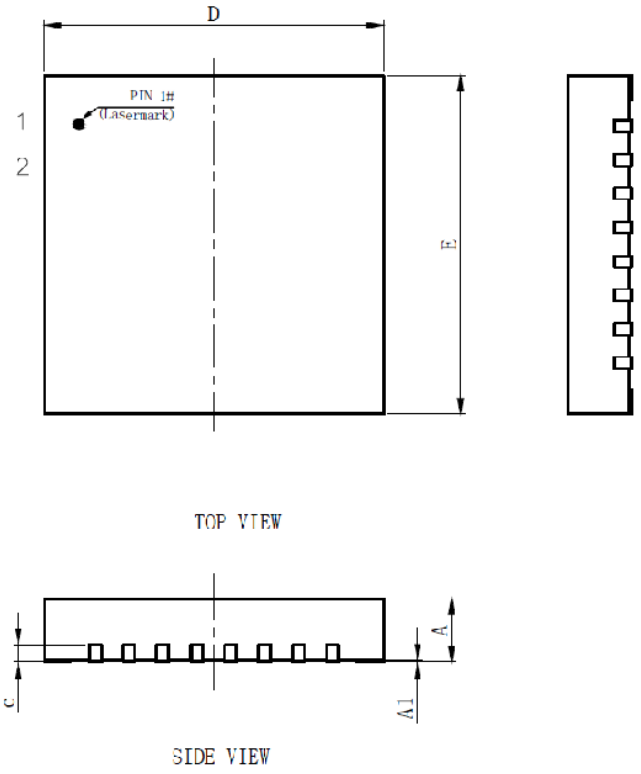
GPIO Muxing Table

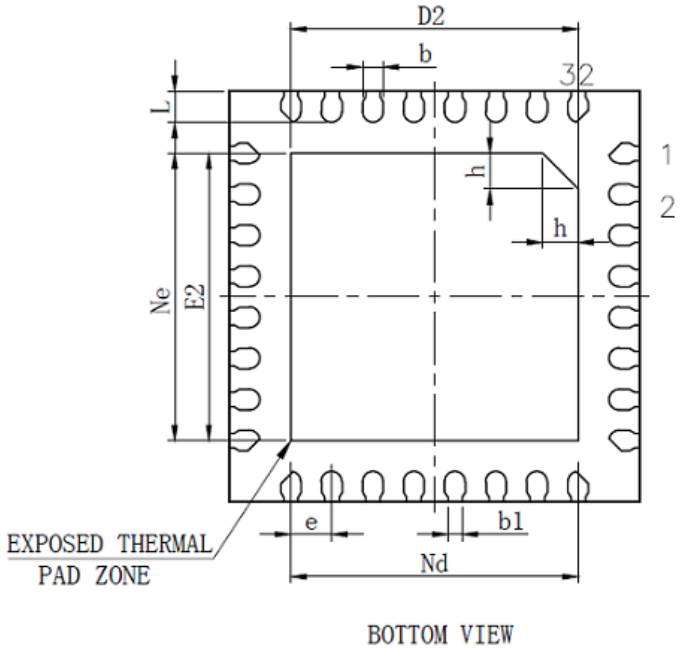
GPIOs	Function1	Function2
GPIO[0]		
GPIO[1]		
GPIO[2]		
GPIO[3]		
GPIO[4]		
GPIO[5]		
GPIO[6]	EXEN	
GPIO[7]		
GPIO[8]		
GPIO[9]		
GPIO[10]		
GPIO[11]		
GPIO[12]		
GPIO[13]		

GPIO[14]		
GPIO[15]		
GPIO[16]		
GPIO[17]		adc0
GPIO[18]		adc1
GPIO[19]		
GPIO[20]		adc2
GPIO[21]		adc3
GPIO[22]		adc4
GPIO[23]	SPI-IO2	adc5
GPIO[24]	SPI-IO1	adc6
GPIO[25]	SPI-NCS	adc7
GPIO[26]	SPI-IO3	
GPIO[27]	SPI-SCK	wakeup1
GPIO[28]	SPI-IO0	wakeup2
GPIO[29]	SDA	
GPIO[30]	SCL	
GPIO[31]		
GPIO[32]		
GPIO[33]		
GPIO[34]		
GPIO[35]		
GPIO[36]		
GPIO[37]		
GPIO[38]		
GPIO[39]		

Note: Drive capability of GPIO[20:40] is up to 100mA, other GPIO's drive capability is 10mA;Micbias output 1.5-2.8V@3mA.

Package Physical Dimension (QFN4x4_32L)

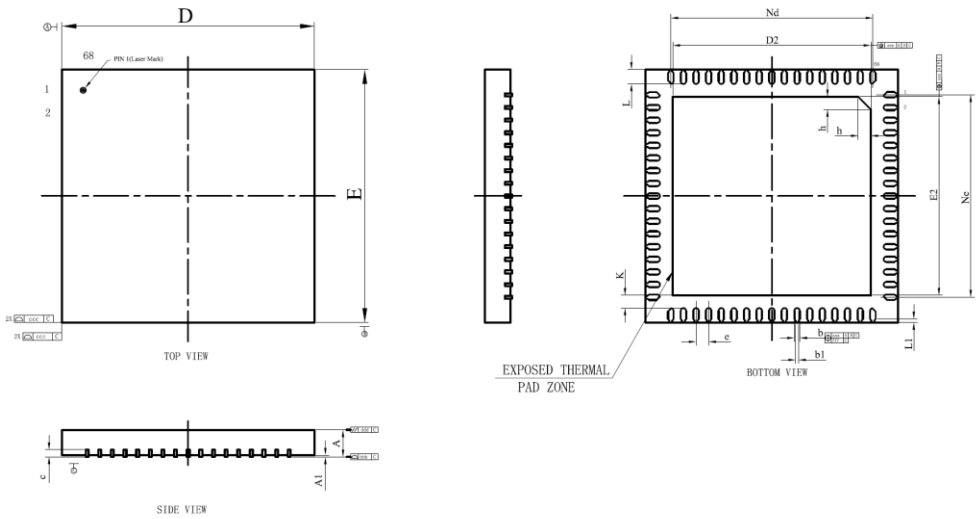




BOTTOM VIEW

SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0. 70	0.75	0. 80	
	0. 80	0.85	0. 90	⚠2
	0. 85	0.90	0. 95	⚠1
A1	0	0.02	0. 05	
b	0. 15	0.20	0. 25	
b1	0. 14REF			
c	0. 18	0.20	0. 25	
D	3. 90	4. 00	4. 10	
D2	2. 70	2. 80	2. 90	
e	0. 40BSC			
Ne	2. 80BSC			
Nd	2. 80BSC			
E	3. 90	4. 00	4. 10	
E2	2. 70	2. 80	2. 90	
L	0. 25	0.30	0. 35	
h	0. 30	0. 35	0. 40	
L/F载体尺寸	122X122			

Package Physical Dimension (QFN7x7_68L)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.10	0.15	0.20
b1	0.08REF		
c	0.18	0.20	0.25
D	6.90	7.00	7.10
D2	5.39	5.49	5.59
e	0.35BSC		
Nd	5.60BSC		
E	6.90	7.00	7.10
E2	5.39	5.49	5.59
Ne	5.60BSC		
L	0.35	0.40	0.45
L1	0.10REF		
K	0.20	—	—
h	0.30	0.35	0.40
aaa	0.07		
bbb	0.08		
ccc	0.10		
ddd	0.10		
eee	0.10		
fff	0.05		
L/F载体尺寸 (mil)	232*232		