YC13XX

High Performance Low Power BR/BLE 5.2 SoC

Preliminary Datasheet

General Descriptions

The YC13XX is a high performance, low power System-on-Chip (SoC) integrating a Bluetooth® 5.2 compliant 2.4-GHz transceiver, 24 MHz proprietary 32 bit MCU with a RAM of 12 KB and eFuse of 512 bits.

The YC13XX supports Bluetooth Basic Rate, Bluetooth Low Energy and Bluetooth 5.2 features including high-throughput 2 Mbps, Long Range and the Direction Finding. It can be paired through HCI interface with a more powerful MCU for applications requiring advanced wireless connectivity.

The fully-featured multiprotocol radio, +12 dBm output power, -99 dBm sensitivity and extended temperature range of -40 to 110°C makes it suitable for lighting applications.

The YC13XX features built-in USB, proprietary 32-bit MCU clocked at 24 MHz, integrated capless LDOs supporting 1.7-5.5V supply range, making it a perfect microcontroller for cost-sensitive applications such as mouse devices, toys and disposables.

Key Features

- MCU subsystems
  - 24 MHz 32-bit proprietary MCU for system control and PHY/link layer management
  - AES128 HW encryption
  - Serial wire debug
- Memories
  - 512 bit eFuse
  - 12 kB date RAM
  - 4 kB RAM supporting retention mode
- Radio transceiver
  - BR/Bluetooth 5.2/Long Range
  - +12 dBm TX power in 1dB/steps
  - -99 dBm RX sensitivity @ BLE 1 Mbps
  - -96 dBm RX sensitivity @ BLE 2 Mbps
  - Integrated balun with single-ended output and direct connection to antenna
  - 5.8 mA RX system current @ BLE 1 Mbps -99 dBm sensitivity (3V DC-DC 90% efficiency)
  - 5.2 mA RX system current @ BLE 1 Mbps -97 dBm sensitivity (3V DC-DC 90% efficiency)
  - 10.9 mA TX system current (3V DC-DC 90% efficiency, 0 dBm)
- Power management
  - Always-On (AON) supply: 1.7~ 5.5V
  - Main supply: 1.3 ~ 5.5V supporting external DCDC through a dedicated wakeup pin
  - Integrated LDOs requiring no external decoupling capacitors
  - 3.3V 40 mA capless LDO
  - 1.3 µA in sleep mode (wake on RTC, no RAM retention)
  - 2 µA in sleep mode (wake on RTC, 4 KB RAM retention)
- Clock generation
  - Dedicated PLL to support 16M/24M/26M/32M crystals
  - Crystal trimming
  - 40 MHz RC oscillator for fast wakeup
  - Low jitter low power 32 KHz RC oscillator
- 10-channel 10-bit ADC
- Digital peripherals
  - Up to 20 GPIOs w/ functions fully multiplexed
  - Two-wire master (I^2C compatible) up to 600 kbps
  - 2 x UART(RTS/CTS) with HCI-H5 protocol up to 3.25 Mbps
  - 2 x SPI Master/Slave up to 24 Mbps
  - 1-axis Quadrature Decoder
  - 12 Mbps Full Speed USB 2.0
- Temperature range: -40°C to +110°C

Applications

- Mouse devices
- Toys
- Lightning applications
- Disposables
- Commercial and industrial applications requiring advanced connectivity

Key Benefits

- Best-in-class sensitivity and output power for RF-demanding applications
- BR for enhanced interoperability
- Lowest system cost for cost-oriented designs

Revision History

Version	Date	Owner	Note
0.1	3/15/2021	JH	Initial version
0.2	4/21/2021	JH	Update power consumption data
0.3	5/12/2021	Iris.li	Update Package Information

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1 Block Diagram

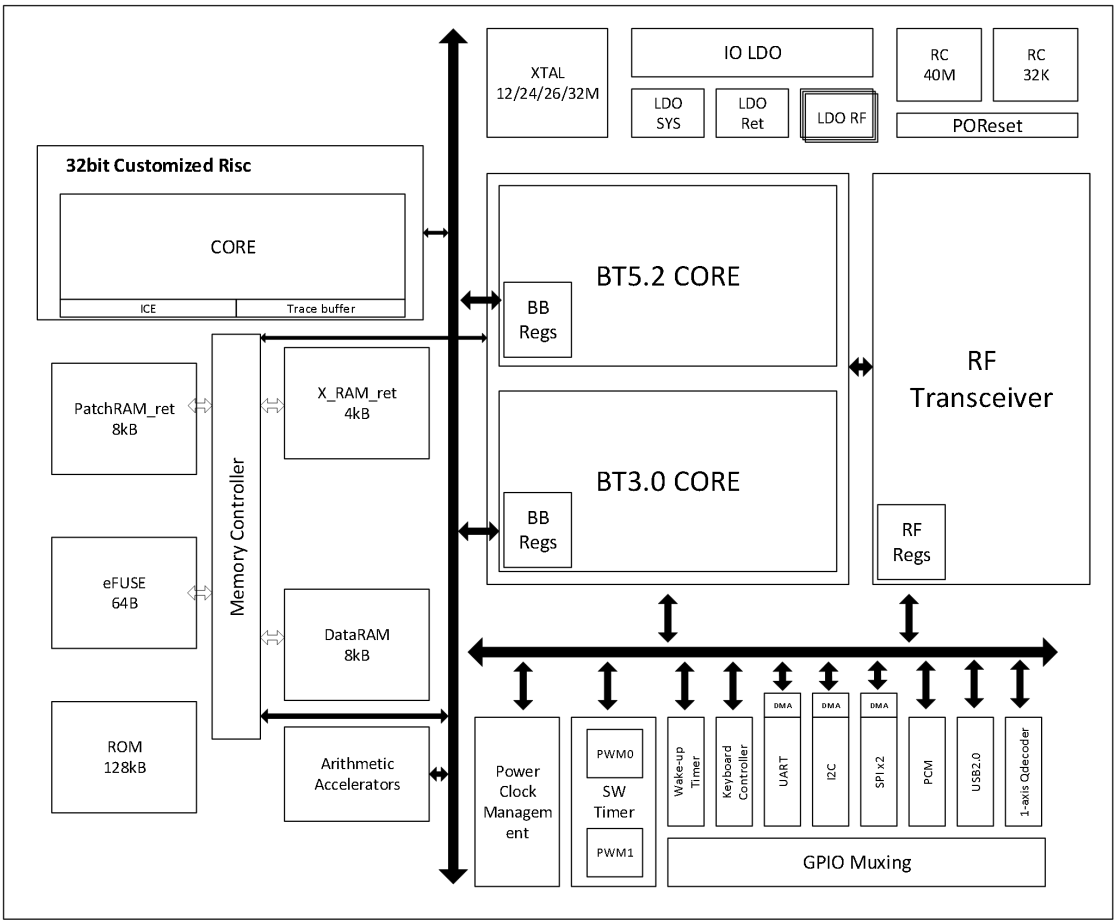


Figure 1- 1 Block diagram

2 Pinout Information

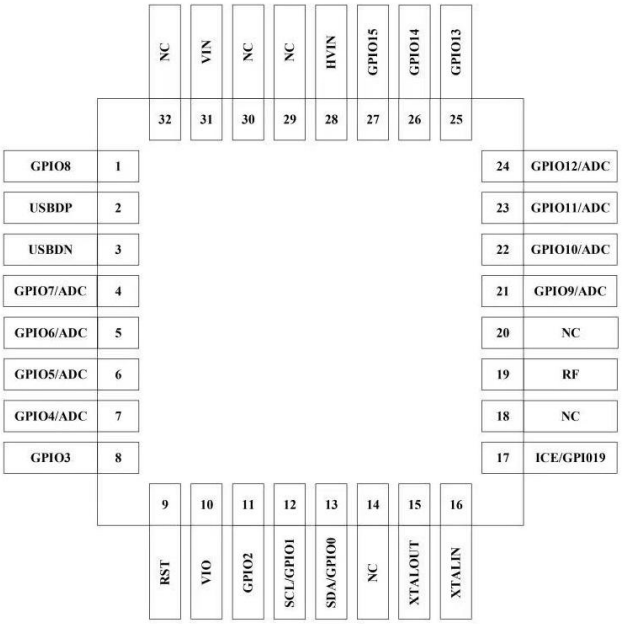


Figure 2- 1 Pinout top view (QFN32 package)

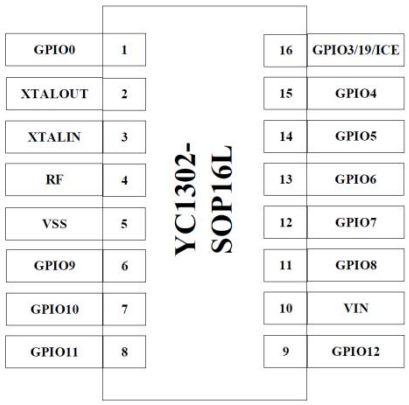


Figure 2- 2 Pinout top view (SOP16 package)

Abbreviations:

PWR: Power pin

AIO: Analog IO pin

DIO: Digital IO pin

RF: RF IO pin

Table 2- 1 Pinout Information

Pin Number		Type	Name	Description
QFN32	SOP16			
1			GPIO8	Refer to Table 2- 2
2		DIO	USBDP	USB port.
3		DIO	USBDN	USB port.
4	12	DIO	GPIO7/ADC	Refer to Table 2- 2
5	13	DIO	GPIO6/ADC	
6	14	DIO	GPIO5/ADC	
7		DIO	GPIO4/ADC	
8		DIO	GPIO3	
9		DIO	RSTN	Global reset, active low. OR gated with internal POR. NC if not needed.
10		PWR	VIO	I/O power, 1.8~3.6V, no external capacitor needed
11	15	DIO	GPIO2	Refer to Table 2- 2
12		DIO	GPIO1/SCL	Internal pull up 1Kohm to VIO and no need external pull up resistor.
13	1	DIO	GPIO0/SDA	Internal pull up 1Kohm to VIO and no need external pull up resistor.
14			NC	
15	2	AIO	XTALOUT	XTAL port
16	3	AIO	XTALIN	XTAL port, or external reference clock input
17	16	DIO	ICE/GPIO19	debug port, Tx & Rx
18			NC	
19	4	RF	RF	ANT port
20			NC	NC
21	6	DIO	GPIO9/ADC/EXEN	Refer to Table 2- 2
22	7	DIO	GPIO10/ADC	
23	8	DIO	GPIO11/ADC	
24	9	DIO	GPIO12/ADC	
25		DIO	GPIO13	
26		DIO	GPIO14	
27		DIO	GPIO15	
28		PWR	HVIN	Always-on power input, 1.55~5.5V, 1μF bypass cap
29			NC	
30			NC	
31	10	PWR	VIN	Main power input, 1.25~5.5V, 1μF bypass cap
32			NC	
	5	GND	VSS	GND
	11	DIO	GPIO8	Refer to Table 2- 2

Note 1 : Drive capability of GPIO[19:2] is up to 100mA,GPIO[1:0] internal pullup & pulldown resistance is 1kohm.

Note 2 : GPIO[9] is by default not gpio function, and is in output high level status after por, which is used as external BUCK enable signal. GPIO[9] will restore gpio function by setting lpm_ctrl[52] to 0.

Note 3 : GPIO[9] can not used as lpm wakeup source.

Note 4 : GPIO[19] is by default in pullup status as ice function after por. GPIO[19] will restore gpio function by setting ice_mode to 0.

Table 2- 2 GPIO Multiplexing

Pin Name	boot function	function-analog
GPIO[0]		atest[5]
GPIO[1]		atest[4]
GPIO[2]		atest[7]
GPIO[3]		atest[6]
GPIO[4]		saradc [0]
GPIO[5]		saradc [1]
GPIO[6]		saradc [2]
GPIO[7]		saradc [3]
GPIO[8]		
GPIO[9]	EXEN	saradc [4]
GPIO[10]		saradc [5]
GPIO[11]		saradc [6]
GPIO[12]		saradc [7]
GPIO[13]		
GPIO[14]		
GPIO[15]		atest[1]
GPIO[16]		atest[0]
GPIO[17]		atest[3]
GPIO[18]		atest[2]
GPIO[19]	ICE	

3 Specifications

3.1 Recommended Operating Conditions

Table 3- 1 Recommended Operation Condition

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage for pin VBAT	V_{BAT}		1.55		5.5	V
Supply voltage for pin VDCDC	V_{DCDC}		1.25		5.5	V
Supply voltage for pin VIO	V_{IO}	VIO supplied by a host chip not VDD33	1.62		3.6	V
Ambient temperature	T_A		-40		110	°C

3.2 Power Consumption

Table 3- 2 Power Consumption Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sleep						
Current through pin VBAT	I_{VBAT_SLEEP}	V_{BAT} = 3.0V		1.3		μA
	$I_{VBAT\_SLEEP\_RET}$			2.0		μA
Current through pin VDCDC	I_{VDCDC_SLEEP}	V_{DCDC} = 1.3V		20.0		nA
RX mode 1 Mbps BLE @ -99 dBm sensitivity						
Current through pin VBAT	I_{VBAT_TX}	V_{BAT} = 3.0V		0.48		mA
Current through pin VDCDC	I_{VDCDC_TX}	V_{DCDC} = 1.3V		11.0		mA
RX mode 1 Mbps BLE @ -97 dBm sensitivity						
Current through pin VBAT	I_{VBAT_TX}	V_{BAT} = 3.0V		0.48		mA
Current through pin VDCDC	I_{VDCDC_TX}	V_{DCDC} = 1.3V		9.9		mA
TX mode 0 dBm						
Current through pin VBAT	I_{VBAT_TX}	V_{BAT} = 3.0V		0.48		mA
Current through pin VDCDC	I_{VDCDC_TX}	V_{DCDC} = 1.3V		18.0		mA

3.3 Radio

All parameters are referred to chip port and measured on the condition of VBAT = VIN = 3.0V if not stated otherwise.

Table 3- 3 Transmitter Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	f_{TX}		2380		2520	MHz
Output power	P_{out}		-18.0		12.0	dBm
Power control step	P_{step}	For part-to-part power calibrations	0.5	1.0		dB
2nd harmonic power	P_{2harm}	0 dBm		-34.0		dBm
		4 dBm		-30.0		dBm
		12 dBm		-22.5		dBm
3rd harmonic power	P_{3harm}	0 dBm				dBm
		4 dBm				dBm
		12 dBm				dBm
4th harmonic power	P_{4harm}	0 dBm				dBm
		4 dBm				dBm
		12 dBm				dBm
Spurious emissions (@ 4 dBm)	P_{spur}	30 MHz to 1000 MHz		-43.7		dBm
		1 GHz to 12.75 GHz		-31.0		dBm
		47 MHz to 74 MHz				dBm
		87.5 MHz to 108 MHz				dBm

		174 MHz to 230 MHz				dBm
		470 MHz to 862 MHz		-44.0		dBm
BDR DH1						
Average frequency deviation	$\Delta f1_{avg\_BR}$	0 dBm		158.7		KHz
		4 dBm		156.8		KHz
		11 dBm		160.8		KHz
Average frequency deviation ratio	$\Delta f2_{avg\_BR}/\Delta f1_{avg\_BR}$	0 dBm	0.8	0.89		
		4 dBm	0.8	0.91		
		11 dBm	0.8	0.84		
Adjacent channel power (4 MHz offset)	P_{adj_BR}	0 dBm	-20.0	-53.57		dBm
		4 dBm	-20.0	-50.46		dBm
		11 dBm	-20.0	-41.49		dBm
Alternate adjacent channel power (6 MHz offset)	P_{aadj_BR}	0 dBm	-30.0	-57.37		dBm
		4 dBm	-30.0	-54.67		dBm
		11 dBm	-30.0	-44.5		dBm
1 Mbps BLE						
Average frequency deviation	$\Delta f1_{avg,\ 1M}$	0 dBm		250.2		KHz
		4 dBm		250.2		KHz
		12 dBm		251.9		KHz
Average frequency deviation ratio	$\Delta f2_{avg\_1M}/\Delta f1_{avg\_1M}$	0 dBm	0.8	0.93		
		4 dBm	0.8	0.94		
		12 dBm	0.8	0.97		
Adjacent channel power (2 MHz offset)	P_{adj_1M}	0 dBm	-20.0	-52.6		dBm
		4 dBm	-20.0	-49.0		dBm
		12 dBm	-20.0	-39.9		dBm
Alternate adjacent channel power (4 MHz offset)	P_{aadj_1M}	0 dBm	-30.0	-57.3		dBm
		4 dBm	-30.0	-54.4		dBm
		12 dBm	-30.0	-45.1		dBm
2 Mbps BLE						
Average frequency deviation	$\Delta f1_{avg\_2M}$	0 dBm		499.7		KHz
		4 dBm		500.7		KHz
		12 dBm		500.3		KHz
Average frequency deviation ratio	$\Delta f2_{avg\_2M}/\Delta f1_{avg\_2M}$	0 dBm	0.8	0.86		
		4 dBm	0.8	0.87		
		12 dBm	0.8	0.86		
Adjacent channel power (4 MHz offset)	P_{adj_2M}	0 dBm	-20.0	-40.9		dBm
		4 dBm	-20.0	-36.6		dBm
		12 dBm	-20.0	-27.8		dBm
Alternate adjacent channel power (6 MHz offset)	P_{aadj_2M}	0 dBm	-30.0	-53.0		dBm
		4 dBm	-30.0	-46.7		dBm
		12 dBm	-30.0	-39.6		dBm

Table 3- 4 Receiver Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	f_{RX}		2380		2520	MHz
Out-of-band blocking	OOB	30 MHz – 2000 MHz	-30			dBm
		2003 – 2399 MHz	-35			dBm
		2484 – 2997 MHz	-35			dBm
		3000 MHz – 12.75 GHz	-30			dBm
Basic Rate						
RX sensitivity	P_{SENS_BR}	0.1 % BER		-94.5	-70	dBm
C/I co-channel	C/I_{CO_BR}	0.1 % BER		1.1	11	dB
C/I 1 MHz adjacent channel	C/I_{1_1M}	0.1 % BER		-32.3	0	dB
C/I 2 MHz adjacent channel	C/I_{2_1M}	0.1 % BER		-43.6	-30	dB
C/I ⩾3 MHz adjacent channel	C/I_{3_1M}	0.1 % BER		-46.0	-40	dB
C/I image channel	C/I_{im_1M}	0.1 % BER		-21.0	-9	dB
C/I image channel + 1MHz	C/I_{im+1_1M}	0.1 % BER		-30.0	-20	dB
Maximum input signal level	$P_{IN\_MAX\_1M}$	0.1 % BER		0.0	-20	dBm
1 Mbps BLE						
RX sensitivity	P_{SENS_1M}	0.1 % BER		-99.5	-70	dBm
C/I co-channel	C/I_{CO_1M}	0.1 % BER		3.8	21	dB
C/I 1 MHz adjacent channel	C/I_{1_1M}	0.1 % BER		-23.6	15	dB
C/I 2 MHz adjacent channel	C/I_{2_1M}	0.1 % BER		-26.8	-17	dB
C/I ⩾3 MHz adjacent channel	C/I_{3_1M}	0.1 % BER		-37.9	-27	dB
C/I image channel	C/I_{im_1M}	0.1 % BER		-16.3	-9	dB
C/I image channel + 1MHz	C/I_{im+1_1M}	0.1 % BER		-19.5	-15	dB
Maximum input signal level	$P_{IN\_MAX\_1M}$	0.1 % BER		0.0	-10	dBm

3.4 24 MHz Crystal Oscillator

Table 3- 5 24 MHz Crystal Oscillator Characteristic

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal frequency	f_{XTAL}		16	24	32	MHz
Crystal frequency tolerance	Δf_{XTAL}		-50		50	ppm
Load capacitance	$C_{L, INN}$	Programmable via registers		6	12	pF
Phase noise (referred to 24 MHz)	PN_{XTAL}	24 MHz at 100Hz offset		-115		dBc/Hz
		24 MHz at 1KHz offset		-125		dBc/Hz
		24 MHz at 10KHz offset		-135		dBc/Hz
		24 MHz at 100KHz offset		-142		dBc/Hz
		24 MHz at 1MHz offset		-146		dBc/Hz
Duty cycle	DC_{XTAL}		40.0	50.0	60.0	%
Startup time	T_{ST}	Amplitude settles to ±80% its normal value		1.5		mS

3.5 LDO Characteristics

Table 3- 6 LDO Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage range	V_{IN}				5.5	MHz
Output voltage	V_{OUT_SLEEP}	I_{LOAD}=20 mA, when input voltage below 3.3V, output equals input		3.35		V
	V_{OUT_ACTIVE}	I_{LOAD}=100 μA, when input voltage below 3.3V, output equals input		3.35		V
Maximum load current	I_{LOAD}	Active mode		40		mA
Output load capacitance	C_L		0		1	μF
Quiescent current	I_{Q_SLEEP}	doze mode		50		nA
	I_{Q_ACTIVE}	active mode		50		μA

3.6 Reset Characteristics

Reset voltage is monitored on pin VBAT_HIGH.

Table 3- 7 Reset Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset voltage threshold	V_{POR}	rising edge	1.55	1.70	1.85	V
	V_{PDR}	falling edge	1.50	1.65	1.80	V
POR stretch time	T_{POR}			20.00		mS
PDR stretch time	T_{PDR}			20		μS

4 Application Schematic

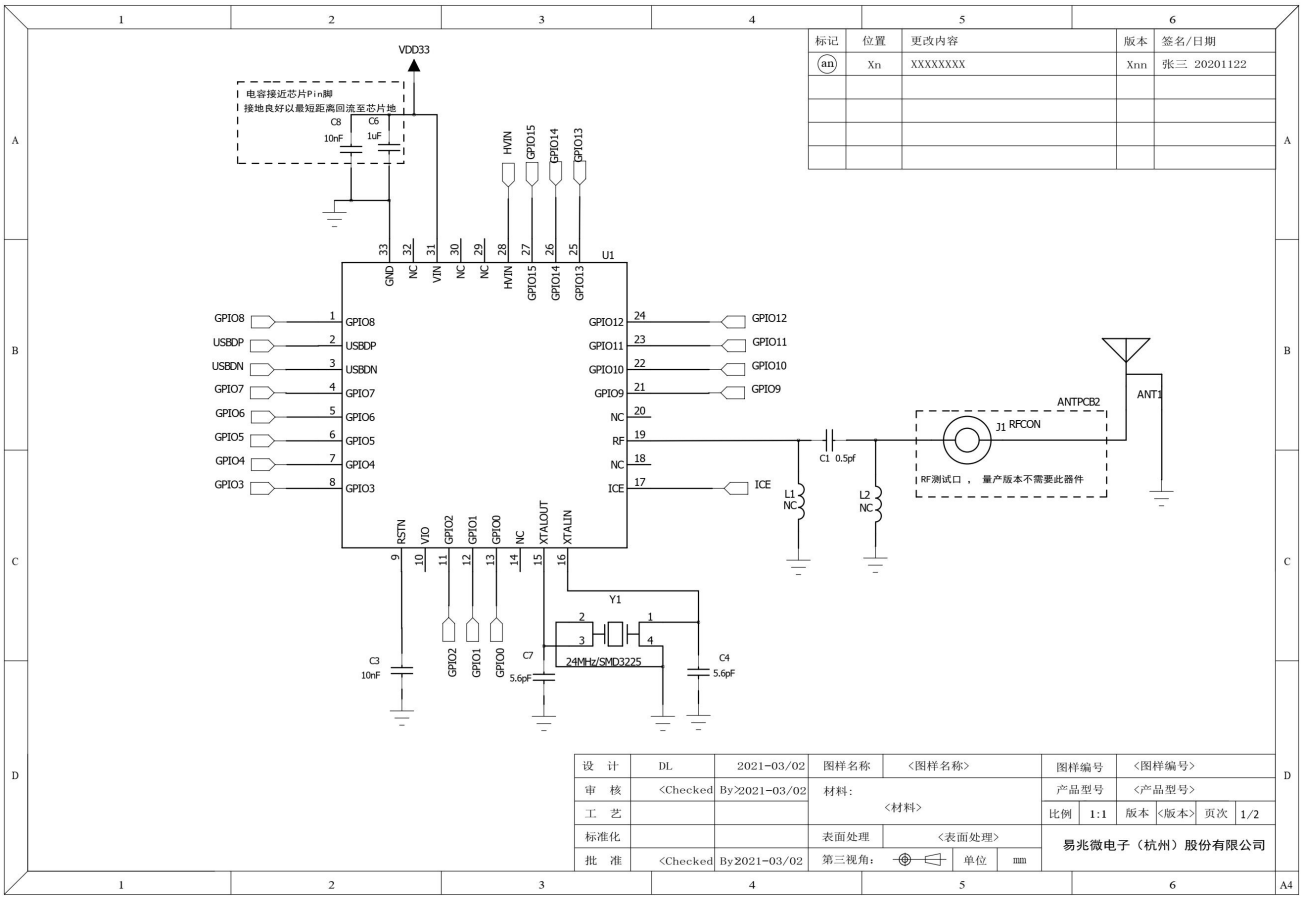


Figure 4- 1 Typical application: QFN 32-pin

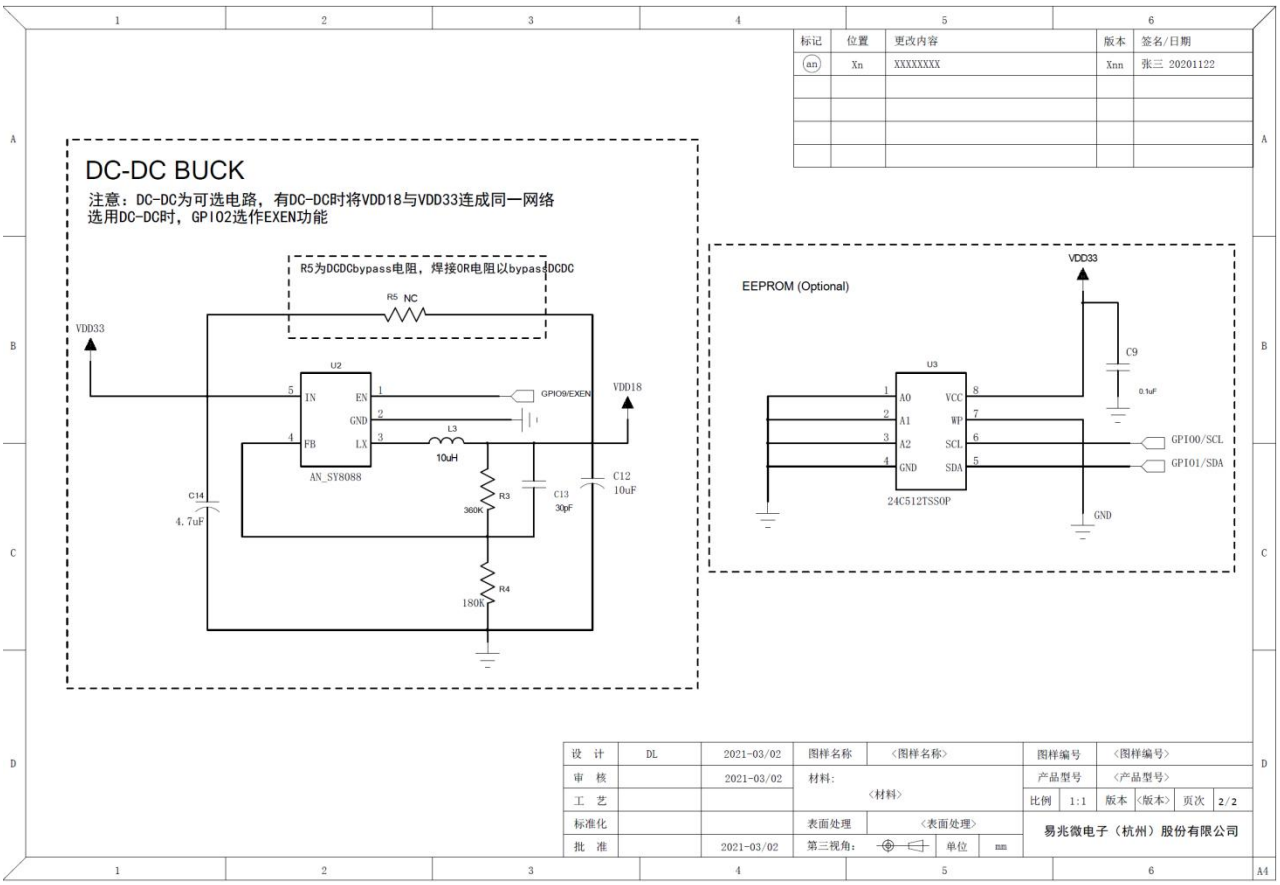
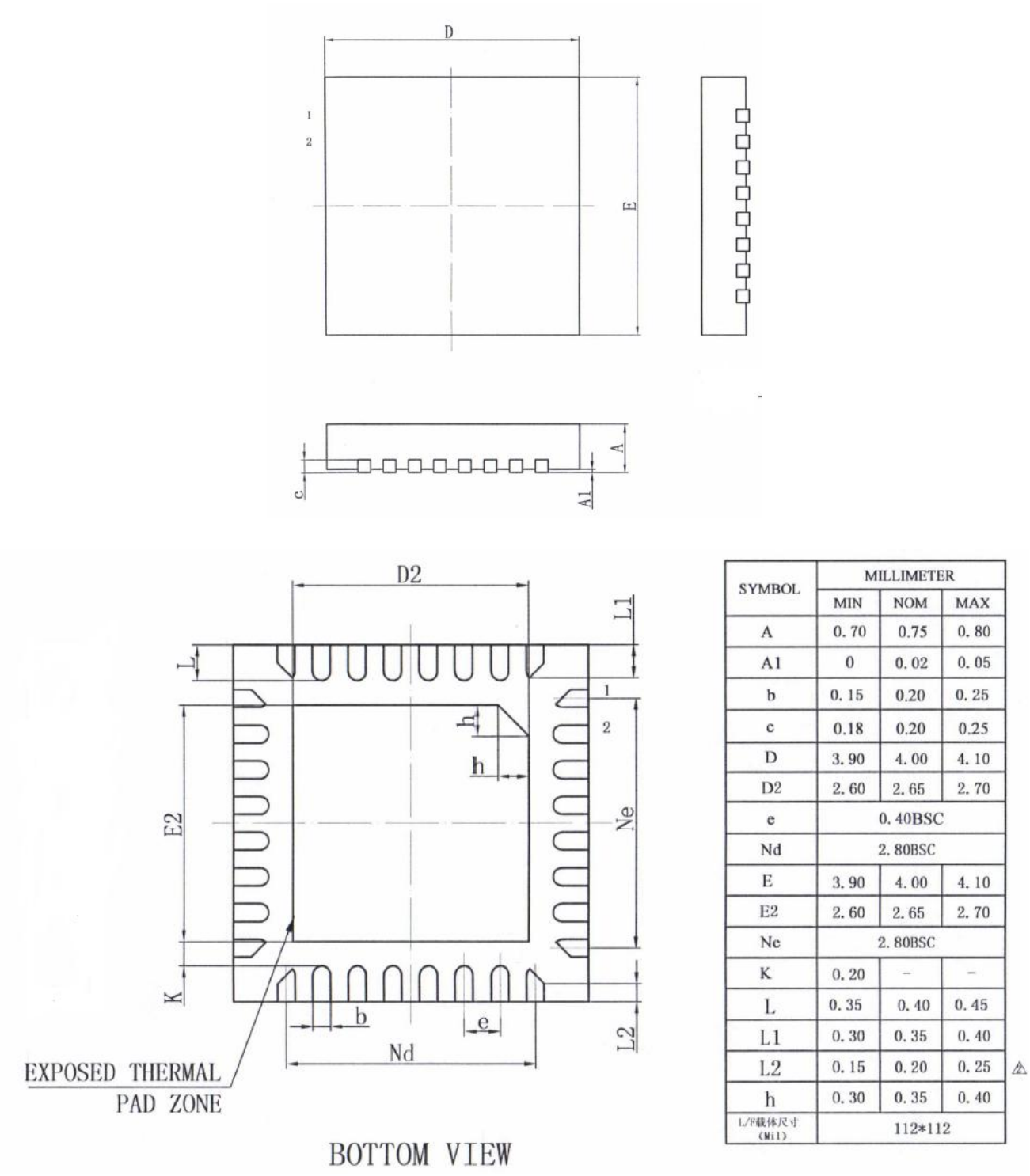


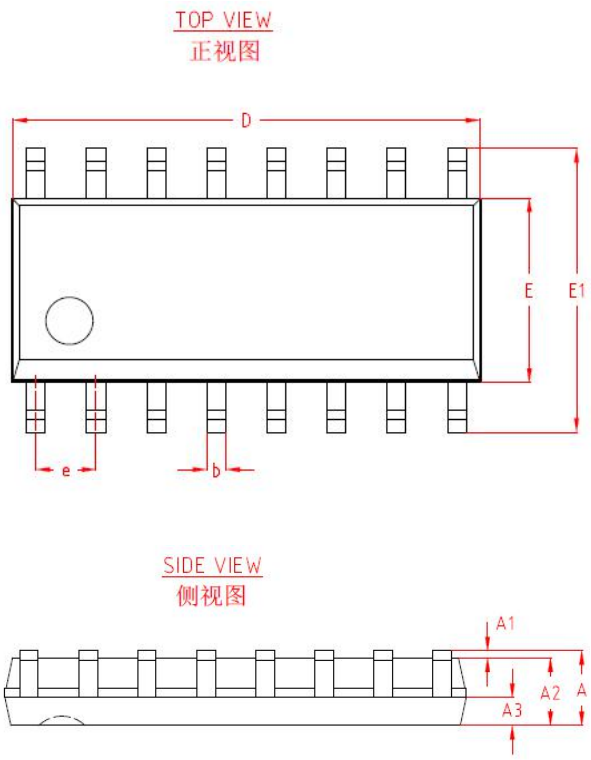
Figure 4- 2 Typical application: SOP 16-pin

5 Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.60	2.65	2.70
e	0.40BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.60	2.65	2.70
Ne	2.80BSC		
K	0.20	–	–
L	0.35	0.40	0.45
L1	0.30	0.35	0.40
L2	0.15	0.20	0.25
h	0.30	0.35	0.40
L/F载体尺寸 (Mil)	112*112		

Figure 5- 1 QFN32 package dimensions



机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	–	–	1.75
A1	0.10	–	0.25
A2	1.35	1.45	1.55
A3	0.60	0.65	0.70
b	0.35	–	0.50
c	0.19	–	0.25
D	9.80	10.00	10.20
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
e	1.27 BSC		
h	0.30	–	0.50
L	0.40	–	0.80
θ	0°	–	8°

Figure 5- 2 SOP16 package dimensions