YC3121 Bluetooth MCU

Product Brief

V1.8

Revision History

Version	Date	Author	Description
V1.0	2018-5-20	Kiwen	Initial version
V1.1	2020-11-24	Iris.li	Remove CHGR module

Confidentiality Level:

Confidential

Contents

1. IC Introduction

1.1. General Description

YC3121 SoC is embedded with 32bit RISC core processor and integrated with Bluetooth 5.0 multi-modes (BR/EDR+BLE). With features such as outstanding structure, high performance and ultra-low power, YC3121 provides high performance secured data process solution.

With embedded hardware security encryption module, YC3121 support several mainstream encryption algorithms, such as DES, TDES, AES, SM2, SM3, SM4, ECC, RSA, SHA and GmSSL. YC3121 is capable to detect multi-attacks and in line with the financial security equipment standards.

Embedded with security BOOT program, YC3121 supports RSA signature verification for firmware when downloading and initialization. YC3121 is embedded with optional 512KB/1024KB secured Flash, 64KB SRAM or 8KB OTP storage area. Integrated with abundant peripheral resources, all YC3121 peripheral software drivers are compatible with the interface of present mainstream security chips so that users are able to speed up developing and porting based on the existing solutions.

1.2. Key Features

- 32-bit RISC Core MCU
  - MPU protection unit
  - Up to 96MHZ clock speed, supporting 2, 4, 8 frequency division
  - One controllable JTAG debug port
- Low power, high performance, highly intergraded Bluetooth 5.0 dual-mode (BR/EDR+BLE)
  - Single-end RFIO

  - -93dBm in BLE mode
  - Supporting 250kbps, 1/2/3Mbps data rates
  - Tx Power up to +6dBm
  - Frequency band ranged from 2400MHz to 2483.5MHz
- 64K Random scrambling SRAM
- 512KB/1MB selectable secured storage Flash
- 8KB OTP
- Secured encryption algorithm acceleration engine
  - Symmetry algorithm: DES, TDES, AES-128/192/256, GM IV (SM4)
  - Asymmetric algorithm: RSA-1024/2048, GM II (SM2) , ECC
  - HASH validation algorithm: SHA-1/224/256/384/512, GM III (SM3)
- One ISO7816 interface, supporting 3V and 1.8V power supply
- One 3-track magnetic stripe card decoding module, supporting standard cards such as ISO/ABA, AAMVA and IBM
- Two UART interfaces
- Two SPI and one QSPI interfaces
- Eight 32bit TIMER (supporting PWM)
- One true random number generator
- One IIC interface
- Six DMA (SPI0, SPI1, UART0, UART1, IIC, MEMCP) modules
- One CRC module
- 48 GPIOs
- Supporting 8 static Tamper or 4-group dynamic Tamper (4 output & 4 input) , and dynamic/static configurable
- One group internal Sensor (supporting sensors such as high/low voltage, high/low temperature, mesh, clock and voltage glitch)
- One key storage area (32x32bits supporting hardware fast deletion)
- One USB interface
- One watch-dog module
- 10bit ADC modules

- HVIN (lithium battery) ADC voltage sampling range: 3~5V
- GPIO (GPIO37~44) ADC voltage sampling range: 0~1.2V

1.3. Applications

Financial security equipment, mobile security equipment and any other security equipment sensitive to power consumption and cost.

1.4. Block Diagram

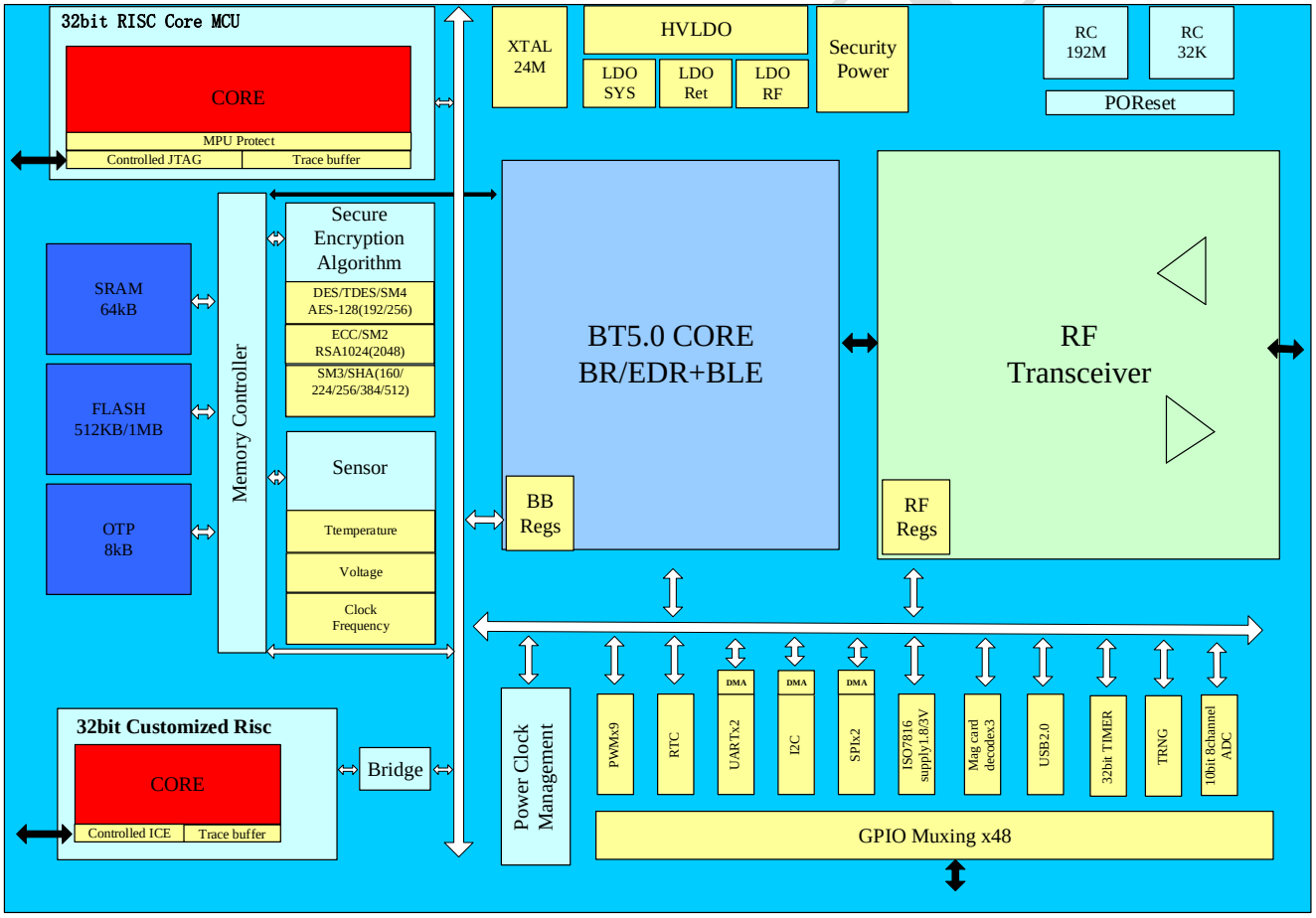


Figure 1. Block Diagram

Electrical Characteristics

Parameter	Description	Range			Unit
		Min	Typ	Max	

2. IC Specifications

2.1. Electrical Characteristics

HVIN	HVLDO Input	3.5	4.2	5.5	V
VIN	Power Supply Input	1.8	3.0	3.6	V
VBAT	Button battery Input	1.9	3.0	3.6	V
VIO	GPIO Power Supply	1.8	3.0	3.6	V
USB Plug-in Detection	USB Plug-in Detection Pin	4.25	5.0	6.5	V
IHVLDO	HVLDO Driving Current	-	-	200	mA
Tamb	Operating Temperature	-40	-	+80	℃
Tstg	Storage Temperature	-40	-	+125	℃
VSS	Ground	-0.3	0	+0.3	V
Voh	Digital Output High Voltage	0.7*VIO	VIO	VIO	V
Vol	Digital Output Low Voltage	VSS	VSS	0.3*VIO	V
Ioh	Drain Current	GPIO[0:7], GPIO[32:47]:25mA ; other:15mA			
Iol	Drive Current	GPIO[0:7], GPIO[32:47]:25mA ; other:15mA			
Vih	Digital Input High Voltage	0.7*VIO	VIO	VIO	V
Vil	Digital Input Low Voltage	VSS	VSS	0.3*VIO	V

Security Characteristics

Sensor	Description	Range	Unit
Temperature Sensor	High Temperature Detection	100±10	℃
	Low Temperature Detection	-30~-40	℃
Voltage Sensor	Main Power Supply High Voltage Detection	3.7±0.15	V
	Main Power Supply Low Voltage Detection	1.5±0.15	V
	Battery Power Supply High Voltage Detection	3.7±0.15	V
	Battery Power Supply Low Voltage Detection	1.5±0.15	V
Clock Frequency Sensor	12MHz Clock Frequency Detection	12±25%	MHz

	32KHz Clock Frequency Detection	32±25%	MHz
External Tamper Resistance	Tamper IO Pull-up Resistance Value	1M±10%	Ω

2.2. Bluetooth RF Characteristics

Name	Parameter (Condition)	Min	Typ	Max	Unit	Comment
Normal RF Condition						
FOP	Operating Frequency	2400		2480	MHz	
FXTAL	Crystal Frequency	12	24	32		(1)
Transmitter Characteristics						
PRF	RF output power	-20	0	6	dBm	
CD	Carrier Drift Rate		5		kHz/50us	
PRF1	Out of band emission 2 MHz (GFSK)		-40		dBm	
PRF2	Out of band emission 3 MHz (GFSK)		-48		dBm	
BW	20dB bandwidth		0.9		MHz	
EVM	Modulation Accuracy, RMS DEVM (π/4 DQPSK)		7	20	%	
	Modulation Accuracy, RMS DEVM (8PSK)		7	13	%	
	Modulation Accuracy, 99% DEVM (π/4 DQPSK)		14	30	%	
	Modulation Accuracy, 99% DEVM (8PSK)		14	20	%	
	Modulation Accuracy, Peak DEVM (π/4 DQPSK & 8PSK)		18	35	%	
	Modulation Accuracy, Peak DEVM (8PSK)		18	25	%	
PRF1	Out of band emission 2 MHz (π/4 DQPSK & 8PSK)		-30	-20		
PRF2	Out of band emission 3 MHz (π/4 DQPSK & 8PSK)		-42	-40		
Receiver Characteristics						
	BT4.0 (BLE)					
SEN	High Gain mode, Sensitivity @0.1%		-93		dBm	
SEN	Standard Gain mode, Sensitivity @0.1%		-87		dBm	
MaxIn	Maximum Input Power		0		dBm	
C/ICO	Co-channel C/I, Basic Rate, GFSK		7		dB	

C/I1ST	ACS C/I 1MHz, Basic Rate, GFSK		5.5	7	dB	
C/I2ND	ACS C/I 2MHz, Basic Rate, GFSK		-36	-34	dB	
C/I3RD	ACS C/I 3MHz, Basic Rate, GFSK		-43		dB	
C/I1STI	ACS C/I Image channel, Basic Rate, GFSK		-34		dB	
C/I2NDI	C/I 1 MHz adjacent to image channel, Basic Rate, GFSK		-28		dB	
	BT3.0 (BR & EDR)					
SEN	Basic Rate, GFSK, BER<0.1%, Dirty Tx on		-90		dBm	
SEN	EDR, π/4 DQPSK, BER<0.01%, Dirty Tx on		-91		dBm	
SEN	EDR, 8PSK, BER<0.01%, Dirty Tx on		-83		dBm	
MaxIn	Maximum Input Power		0		dBm	
C/ICO	Co-channel C/I, EDR, π/4 DQPSK		10.5		dB	
C/I1ST	ACS C/I 1MHz, EDR, π/4 DQPSK		-8		dB	
C/I2ND	ACS C/I 2MHz, EDR, π/4 DQPSK				dB	
C/I3RD	ACS C/I 3MHz, EDR, π/4 DQPSK		-54		dB	
C/I1STI	ACS C/I Image channel, EDR, π/4 DQPSK		-27		dB	
C/I2NDI	C/I 1 MHz adjacent to image channel, EDR, π/4 DQPSK		-43		dB	
C/ICO	Co-channel C/I, EDR, 8PSK		20		dB	
C/I1ST	ACS C/I 1MHz, EDR, 8PSK		0		dB	
C/I2ND	ACS C/I 2MHz, EDR, 8PSK		-20		dB	
C/I3RD	ACS C/I 3MHz, EDR, 8PSK		-45		dB	
C/I1STI	ACS C/I Image channel, EDR, 8PSK		-18		dB	
C/I2NDI	C/I 1 MHz adjacent to image channel, EDR, 8PSK		-33		dB	

(1) 12M, 16M, 24M, 26M, 32M crystal supported, 24M by default

2.3. Power Consumption

Operating Mode	Description	YC3121Power Consumption (including BT)
RUN	1. All Peripherals On	27.35mA (@96M)
	2. All Peripherals Off	7.46mA (@48M)
CPU Sleep	1. All Peripherals Off	2.0mA
Deep Sleep	Support IO Low Level / RTC / Attacking / Charging / Card reading wake-up	2.0uA
VBAT	Test Condition: All Tamper Input Gounded, Main Power Supply Off, All Internal Sensors On	1.4uA

2.4. Pin Definition

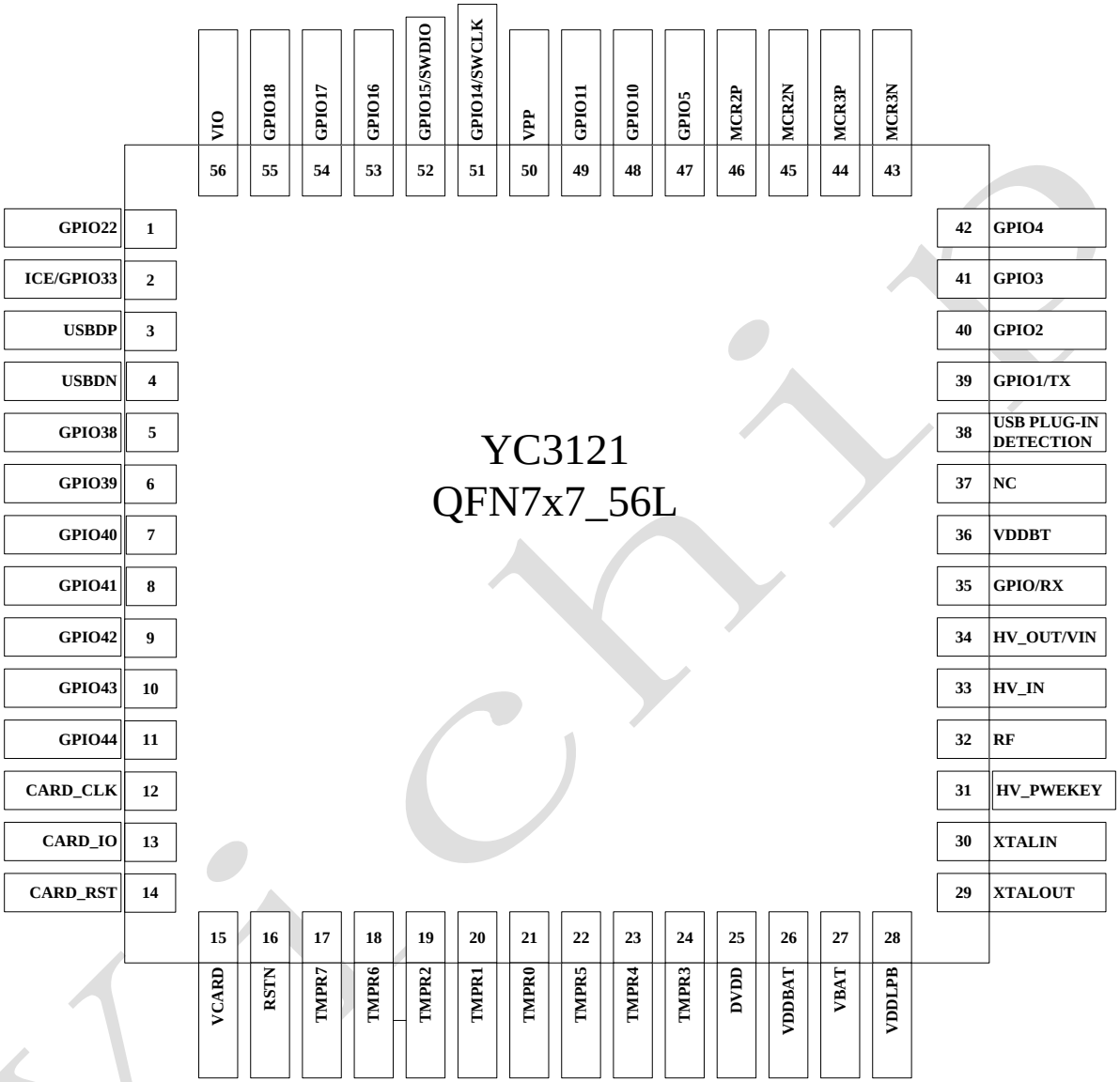


Figure 2. QFN56L IC Pin Assignment

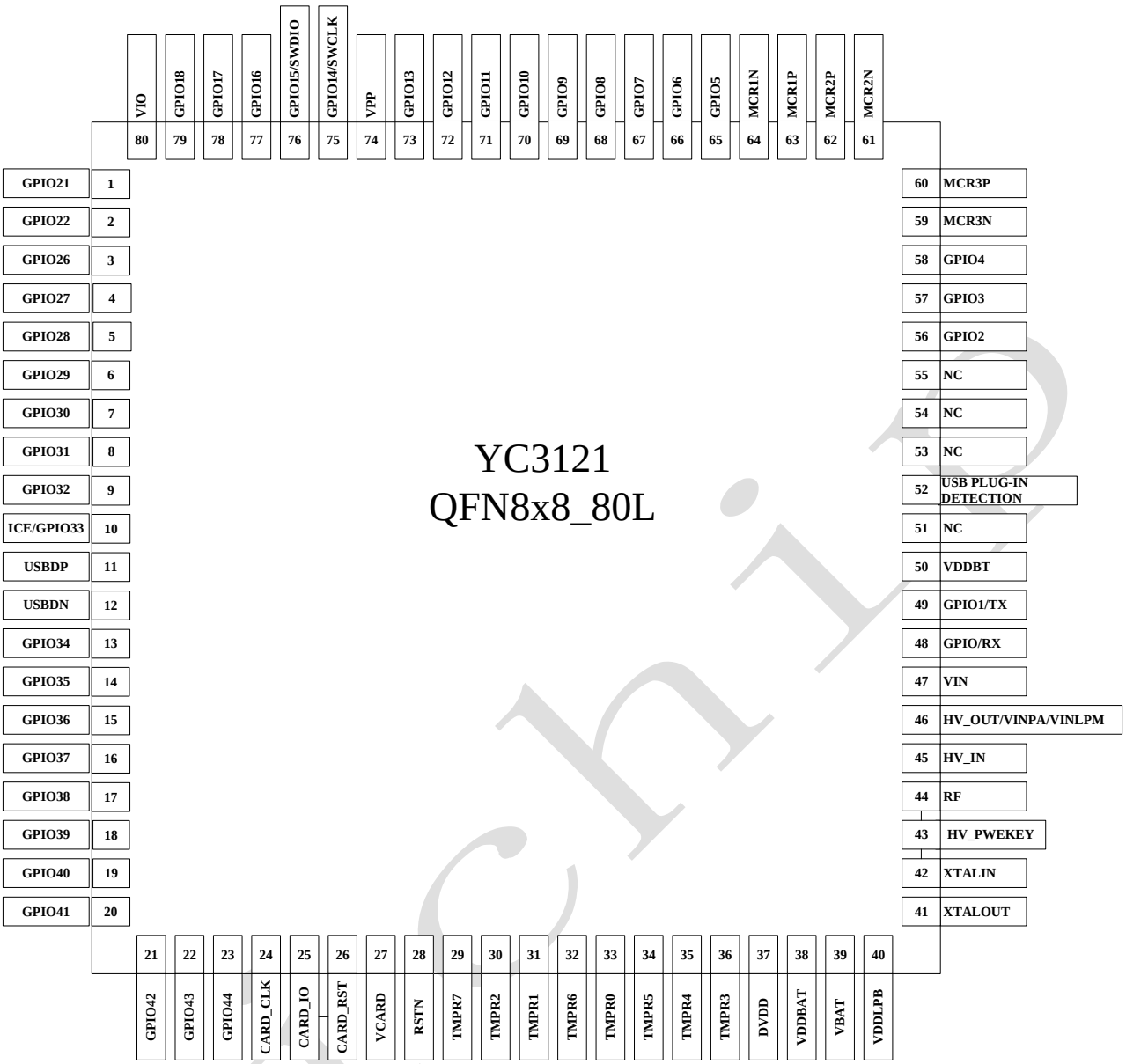


Figure 3. QFN80L IC Pin Assignment

QFN56pin Assignment

PIN No.	Pad name	Description	Reusable Features
1	GPIO22 (PB6)	Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
2	GPIO33/ICE (PC1)	Default ICE，Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
3	USBDP		N/A
4	USBDN		N/A

5	GPIO38 (PC6)	adc_channel1，IO Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
6	GPIO39 (PC7)	adc_channel2，IO Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
7	GPIO40 (PC8)	adc_channel3，IO Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
8	GPIO41 (PC9)	adc_channel4，IO Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
9	GPIO42 (PC10)	adc_channel5，IO Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
10	GPIO43 (PC11)	adc_channel6，IO Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
11	GPIO44 (PC12)	adc_channel7，IO Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
12	CARD_CLK (PC13)	7816 clock	Vcard enabled，Reusable: IIC, UART0~1, SPI0~1, PWM0~8
13	CARD_IO (PC14)	7816 IO (data)	
14	CARD_RST (PC15)	7816 reset	
15	VCARD	7816 VCC (1.8V & 3.0V)	N/A
16	RSTN	IC reset，Low Valid	N/A
17	TMPR7	Anti-removal Tamper Pair Each Other to Enable Separately. In Static Mode: Grounded; In Dynamic Mode: Directly Paired to Use (0-1, 2-3, 4-5, 6-7)	N/A
18	TMPR6		N/A
19	TMPR2		N/A
20	TMPR1		N/A
21	TMPR0		N/A
22	TMPR5		N/A
23	TMPR4		N/A
24	TMPR3		N/A
25	DVDD	To VIN，Main Power Supply LDO Output, With a Capacitor	N/A
26	VDDBAT	To VBAT，Button Battery Power LDO Output, With a Capacitor	N/A

27	VBAT	Button Battery Power supply	N/A
28	VDDLPB	To VINLPB，Bluetooth LE LDO Output, With a Capacitor	N/A
29	XTALOUT		N/A
30	XTALIN	24MHz Crystal	N/A
31	HV_PWRKEY	HVLDO Power Key	N/A
32	RF	Bluetooth RF	N/A
33	HV_IN	HVLDO Input	N/A
34	VIN	IC Power Supply	N/A
35	GPIO0 (PA0) /RX	ROM BOOT UART RX，Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
36	VDDBT	Bluetooth LDO Output, With a Capacitor	N/A
37	NC	NC	N/A
38	USB Plug-in Detection	USB Plug-in Detection Pin	N/A
39	GPIO1 (PA1) /TX	ROM BOOT UART TX，Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
40	GPIO2 (PA2)	Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
41	GPIO3 (PA3)	Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
42	GPIO4 (PA4)	Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
43	MCR3N	Magnetic Track 3N，NC When Not Used	N/A
44	MCR3P	Magnetic Track 3P，NC When Not Used	N/A
45	MCR2N	Magnetic Track 2N，NC When Not Used	N/A
46	MCR2P	Magnetic Track 2P，NC When Not Used	N/A
47	GPIO5 (PA5)	IO Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
48	GPIO10 (PA10)	IO Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
49	GPIO11 (PA11)	Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8

50	VPP	OTP Programming Power Supply Input	N/A
51	GPIO14 (PA14) /SWCLK	Default JTAG_SW_CLK，IO Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
52	GPIO15 (PA15) /SWDIO	Default JTAG_SW_IO，IO Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
53	GPIO16 (PB0)	Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
54	GPIO17 (PB1)	Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
55	GPIO18 (PB2)	Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
56	VIO	GPIO Power Supply	N/A

Note: Each IO can be configured to one of any IO modes (See datasheet for details)

QFN80pin Assignment

PIN No.	Pad name	Description	Reusable Features
1	GPIO21 (PB5)	Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
2	GPIO22 (PB6)	Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
3	GPIO26 (PB10)	Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
4	GPIO27 (PB11)	Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
5	GPIO28 (PB12)	Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
6	GPIO29 (PB13)	Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
7	GPIO30 (PB14)	Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
8	GPIO31 (PB15)	Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
9	GPIO32 (PC0)	Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
10	GPIO33/ICE (PC1)	Default ICE，Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
11	USBDP		N/A
12	USBDN		N/A

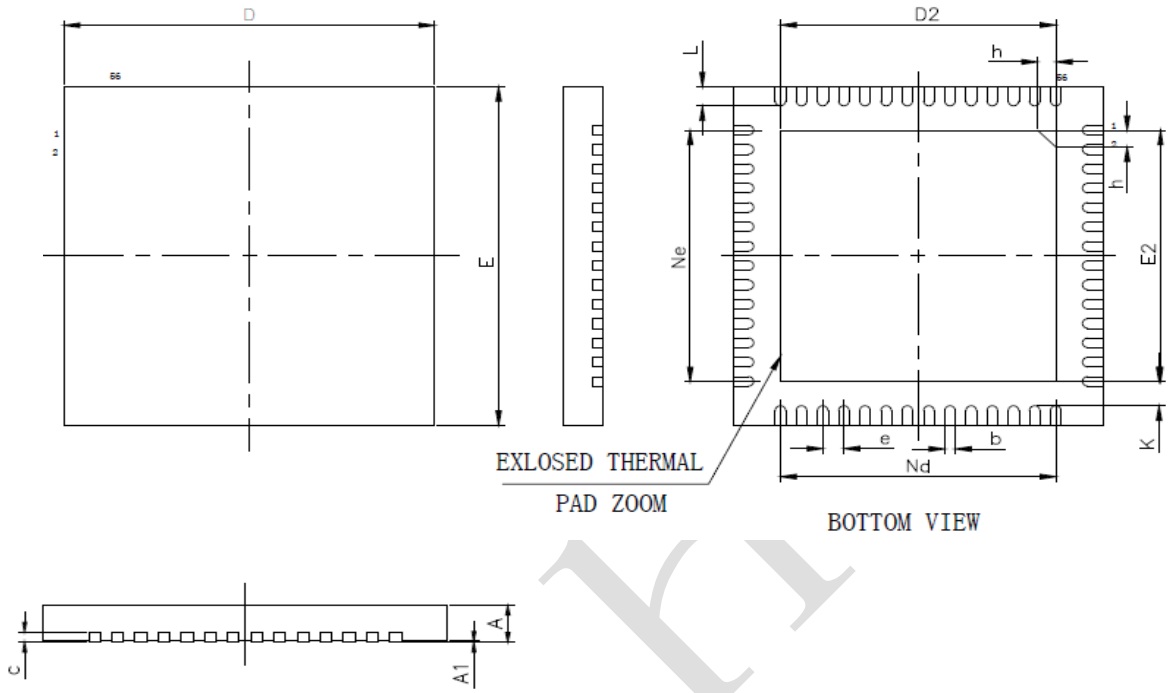
13	GPIO34 (PC2)	IO Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
14	GPIO35 (PC3)	IO Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
15	GPIO36 (PC4)	IO Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
16	GPIO37 (PC5)	adc_channel0，IO Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
17	GPIO38 (PC6)	adc_channel1，IO Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
18	GPIO39 (PC7)	adc_channel2，IO Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
19	GPIO40 (PC8)	adc_channel3，IO Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
20	GPIO41 (PC9)	adc_channel4，IO Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
21	GPIO42 (PC10)	adc_channel5，IO Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
22	GPIO43 (PC11)	adc_channel6，IO Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
23	GPIO44 (PC12)	adc_channel7，IO Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
24	CARD_CLK (PC13)	7816 clock	Vcard enabled，Reusable: IIC, UART0~1, SPI0~1, PWM0~8
25	CARD_IO (PC14)	7816 IO (data)	
26	CARD_RST (PC15)	7816 reset	
27	VCARD	7816 VCC (持 1.8V 和 3.0V)	N/A
28	RSTN	IC reset，Low Valid	N/A
29	TMPR7	Anti-removal Tamper Pair Each Other to Enable Separately. In Static Mode: Grounded; In Dynamic Mode: Directly Paired to Use (0-1, 2-3, 4-5, 6-7)	N/A
30	TMPR2		
31	TMPR1		
32	TMPR6		
33	TMPR0		
34	TMPR5		
35	TMPR4		
36	TMPR3		
37	DVDD	To VIN，Main Power Supply LDO Output, With a Capacitor	N/A
38	VDDBAT	To VBAT，Button Battery Power LDO Output, With a Capacitor	N/A
39	VBAT	Button Battery Power supply	N/A

40	VDDLPB	To VINLPB， Bluetooth LE LDO Output, With a Capacitor	N/A
41	XTALOUT	24MHz Crystal	N/A
42	XTALIN		
43	HV_PWRKEY	HVLDO Power Key	N/A
44	RF	Bluetooth RF	N/A
45	HV_IN	HVLDO Input	N/A
46	HV_OUT/VINPA/ VINLPM	HV_OUT: HVLDO Output (3.3V) ;VINPA: Analog Module Power Supply Input	N/A
47	VIN	IC Power Supply	N/A
48	GPIO0 (PA0) /RX	ROM BOOT UART RX，Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
49	GPIO1 (PA1) /TX	ROM BOOT UART TX，Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
50	VDDBT	Bluetooth LDO Output, With a Capacitor	N/A
51	NC	NC	N/A
52	USB 插入检测	USB Plug-in Detection Pin	N/A
53	NC	NC	N/A
54	NC	NC	N/A
55	NC	NC	N/A
56	GPIO2 (PA2)	Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
57	GPIO3 (PA3)	Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
58	GPIO4 (PA4)	Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
59	MCR3N	Magnetic Track 3N，NC When Not Used	N/A
60	MCR3P	Magnetic Track 3P，NC When Not Used	N/A
61	MCR2N	Magnetic Track 2N，NC When Not Used	N/A
62	MCR2P	Magnetic Track 2P，NC When Not Used	N/A
63	MCR1P	Magnetic Track 1N，NC When Not Used	N/A
64	MCR1N	Magnetic Track 1P，NC When Not Used	N/A

65	GPIO5 (PA5)	IO Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
66	GPIO6 (PA6)	IO Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
67	GPIO7 (PA7)	IO Maximum Driving Current 25mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
68	GPIO8 (PA8)	Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
69	GPIO9 (PA9)	Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
70	GPIO10 (PA10)	Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
71	GPIO11 (PA11)	Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
72	GPIO12 (PA12)	Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
73	GPIO13 (PA13)	Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
74	VPP	OTP Programming Power Supply Input	N/A
75	GPIO14 (PA14) /SWCLK	Default JTAG_SW_CLK，IO Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
76	GPIO15 (PA15) /SWDIO	Default JTAG_SW_IO，IO Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
77	GPIO16 (PB0)	Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
78	GPIO17 (PB1)	Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
79	GPIO18 (PB2)	Maximum Driving Current 15mA	Reusable: IIC, UART0~1, SPI0~1, PWM0~8
80	VIO	GPIO Power Supply	N/A

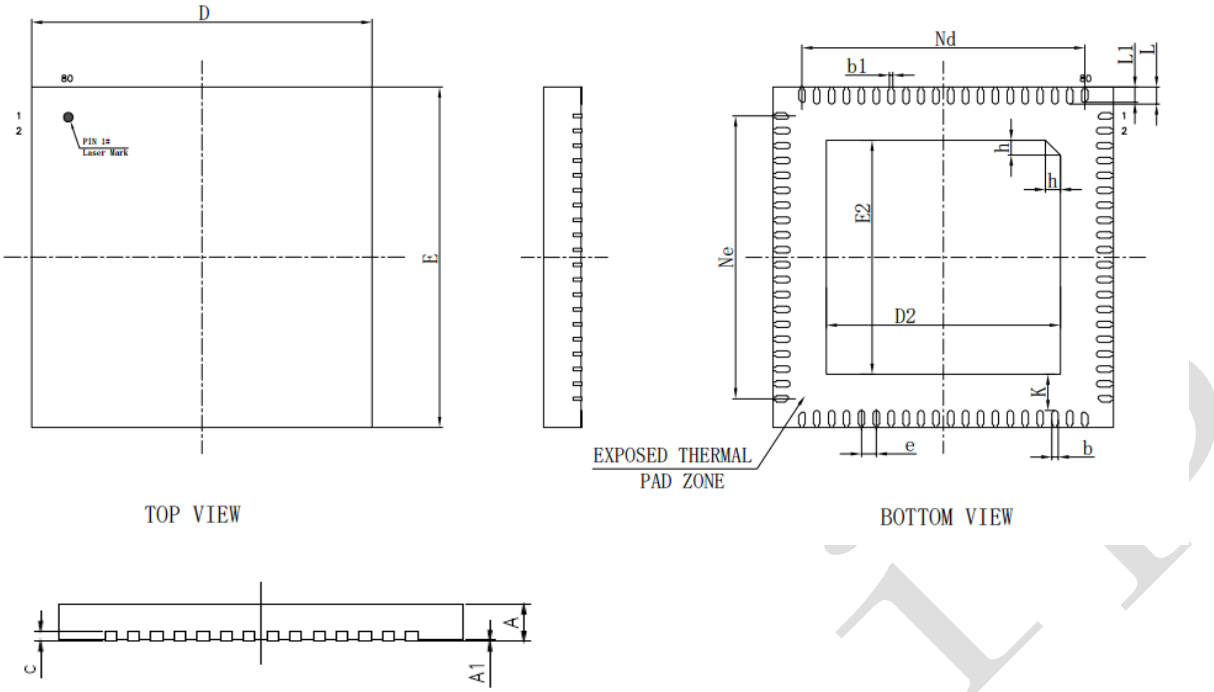
Note: Each IO can be configured to one of any IO modes except ADC channels (See datasheet for details)

2.5. Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
	0.85	0.90	0.95
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	6.90	7.00	7.10
D2	5.10	5.20	5.30
e	0.40BSC		
Nd	5.20BSC		
Ne	5.20BSC		
E	6.90	7.00	7.10
E2	5.10	5.20	5.30
K	0.20	—	—
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F载体尺寸 (mil)	217*217		

Figure 4. QFN56L Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.85	0.90	0.95
A1	0	0.02	0.05
b	0.10	0.15	0.20
b1		0.08REF	
c		0.203REF	
D	7.90	8.00	8.10
D2	5.40	5.50	5.60
e		0.35BSC	
Ne		6.65BSC	
Nd		6.65BSC	
E	7.90	8.00	8.10
E2	5.40	5.50	5.60
L	0.35	0.40	0.45
L1	0.31	0.36	0.41
h	0.30	0.35	0.40
K		0.85REF	

Figure 5. QFN80L Package Information

- IC has one Smart Card Interface;
- Supporting ISO7816-3 standard and EMV Level-1 specifications;
- Supporting asynchronous T=0 & T=1 transport protocols;

3. Peripheral Interface Module Description

3.1. SCI（7816）

- Protocol sequence and timing parameter are configurable;
- Receiving deeply with 8 characters and transmitting with buffer;
- Transceiver with FIFO and interrupt monitoring;
- Register for interrupt status.

3.2. Magnetic Stripe Card Decoder

There is embedded hardware magnetic stripe card decoder module inside the chip, supporting 3 track decoding.

3.3. TIMER

There are 8 embedded 32 bit hardware TIMER modules inside the chip, all including PWM functions.

3.4. GPIO

The chip supports up to 48 GPIO Each IO has reusable pin with peripheral. Each GPIO can be configured to Input, Output and Interrupt modes. The output value can be configured independently for each IO when in output mode. Each IO supports either strong push and pull output or open drain output mode.

3.5. DMA

The chip has 6 DMA modules, including 2 for SPI DMA, 2 for UART DMA, 1 for IIC DMA and 1 for MEMCP DMA.

3.6. SPI

The chip provides 2 SPI interface, supporting master / slave modes. As a master equipment interface, the chip can support to communicate with several slave equipment.

SPI peripheral features:

- Independent address operating for master or slave mode;
- Master mode supporting full duplex, single receiving, single transmitting and EEPROM mode;
- Multi-master conflict detection;
- Supporting 3 wire and 4 wire SPI;
- DMA interface.

Commonly used Motorola SPI communication protocol supports 4 communication modes with full duplex communication capability. Default working mode 0 is adopted during system power up.

SPI Protocol specified 4 communication modes are illustrated below:

- Mode 0: Clock polarity (CPOL) = 0, Clock phase (CPHA) = 0. In this mode, the idle state of the serial sync clock is low level. The chip will take sample at the 1st jumping edge (rising edge) of the serial sync clock. This is the default mode.
- Mode 1: Clock polarity (CPOL) = 0, Clock phase (CPHA) =1. In this mode, the idle state of the serial sync clock is low level. The chip will take sample at the 2nd jumping edge (falling edge) of the serial sync clock.
- Mode 2: Clock polarity (CPOL) = 1, Clock phase (CPHA) =0. In this mode, the idle state of the serial sync clock is high level. The chip will take sample at the 1st jumping edge (falling edge) of the serial sync clock.
- Mode 2: Clock polarity (CPOL) = 1, Clock phase (CPHA) =1. In this mode, the idle state of the serial sync clock is high level. The chip will take sample at the 2nd jumping edge (rising edge) of the serial sync clock.

Note: In order for the chip SPI to work normally, make sure the chip select signal line to keep at high level during the switch of the modes.

SPI Interface is illustrated below:

- SCK: SPI Clock Input pin;
- CSN: SPI Chip Select signal, Input pin with low valid;
- MOSI: SPI Data Input pin;
- MISO: SPI Data Output pin;
- SDIO: Data transport pin for 3 wire SPI

The chip has 2 full duplex UART serial communication interfaces, with fixed clock speed 48MHz. UART

3.7. UART

peripheral features are illustrated below:

- FIFO chip select control；
- Data bit setup, supporting 8/9bit；
- Stop bit setup, supporting 1/2bit；
- Supporting hardware flow control；
- Supporting odd/even verification mode;
- Detection for frame error, verification error, break, interrupt;
- Configurable bytes triggered by interrupt;
- DMA transceiver.

3.8. USB

In conformity with USB 2.0 standard：

- Supporting USB2.0；
- Supporting host negotiates protocol (HNP) and session request protocol (SRP);
- Supporting USB full speed / low speed for SRP;
- Providing 512 byte dedicated RAM and advanced FIFO management;
- Configurable different RAM area for different FIFO through software for flexible & effective RAM use;
- Dynamic allocation for storage area is allowed;
- Unlimited FIFO length (length of 2^n is not enforced and the storage can be used continuously);
- Same node ID is allowed (IN/OUT node can share a FIFO for more efficient use of the storage area);
- EP0-EP34 nodes are available.

3.9. Security Algorithm Module

3.9.1. Security Algorithm Module Introduction

3.9.1. Security Algorithm Introduction

Algorithm module is comprised of:

- Synchronous algorithm: DES, TDES, AES-128/192/256, GM IV (SM4);
- Asynchronous algorithm: RSA-1024/2048, GM II (SM2);
- HASH validation algorithm：SHA-1/224/256/384/512, GM III (SM3);
- True random number generator.

3.9.2. 64 bit High Speed Hardware Public Key Algorithm Engine

- Standalone calculation clock without CPU core: Frequency up to 48MHz;
- Supporting large number (1024/2048 bit) mode multiply / mode power / multiplication computing co-processing;
- Supporting large number (1024/2048 bit) mode inverse computing co-processing;
- Supporting up to 521 ECC point plus, point double, point multiply computing;
- Supporting SM2 algorithm point plus, point double, point multiply computing.

3.9.3. DES/3DES Algorithm Unit

- Supporting DES/3DES algorithm encryption, decryption computing with 2 & 3 key modes;
- Supporting CBC/ECB modes；
- Supporting 160bit/192bit/256bit modes.

3.9.4. SM4 Algorithm Unit

- Supporting CBC/ECB modes.

3.9.5. SHA Algorithm Unit 168

- Supporting SHA160/SHA224/SHA256/SHA384/SHA512.

3.9.6. AES Algorithm Unit

- Supporting 128/192/256 key length.

3.9.7. True Random Number Generator

- Following the related requirements from “Randomness Testing Code” by State Cryptography Administration (SCA);
- Using random number to test international standard FIPS 140-2 and NIST SP800-22 standard test;
- The operating frequency for random number IP can support up to 48MHz.